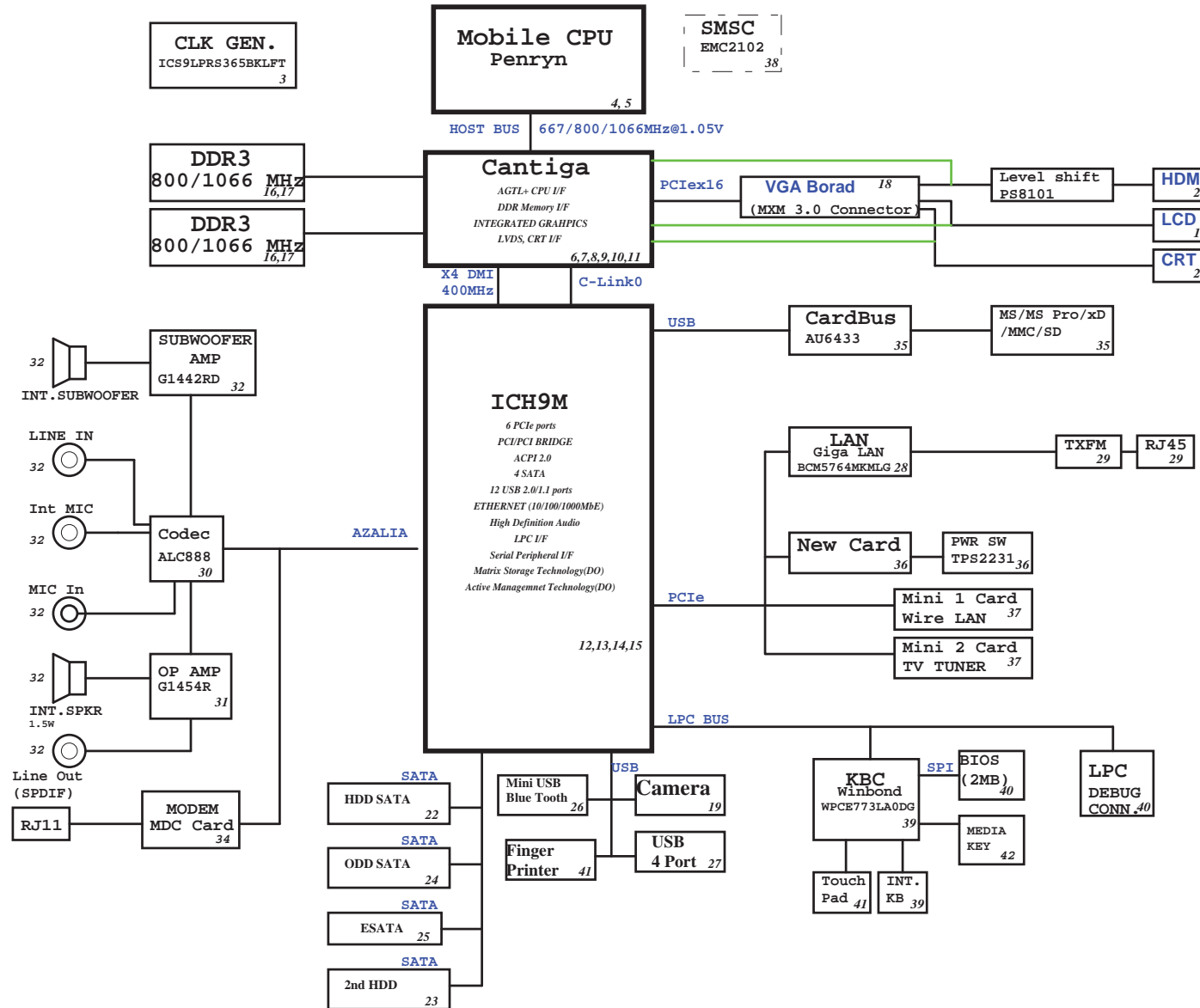


JM70 -MV Block Diagram

Project code: 91.4AN01.001
PCB P/N : 48.4AN01.0SA
REVISION : SB 08246



SYSTEM DC/DC	
ISL62392	46
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5
SYSTEM DC/DC	
TPS51124	46
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A) 1D5V_S3(10A)
RT9026	
1.5V_S3	DDR_VREF_S3 (1.2A)
G9198-15	
3D3V_S5	1D5V_S5 (300mA)
CHARGER	
ISL88731A	50
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC	
ADP3208C	51
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0-1.3V 38A
GFX DC/DC	
ISL6263	48
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0-1.3V 6.5A

PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

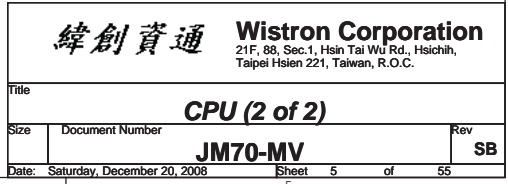
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

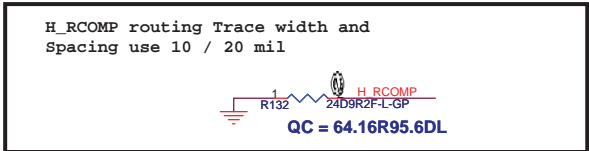
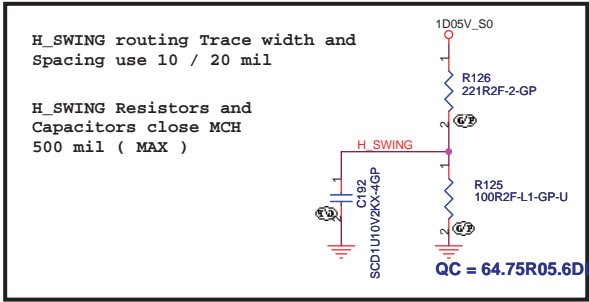
Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operting simulatananeously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

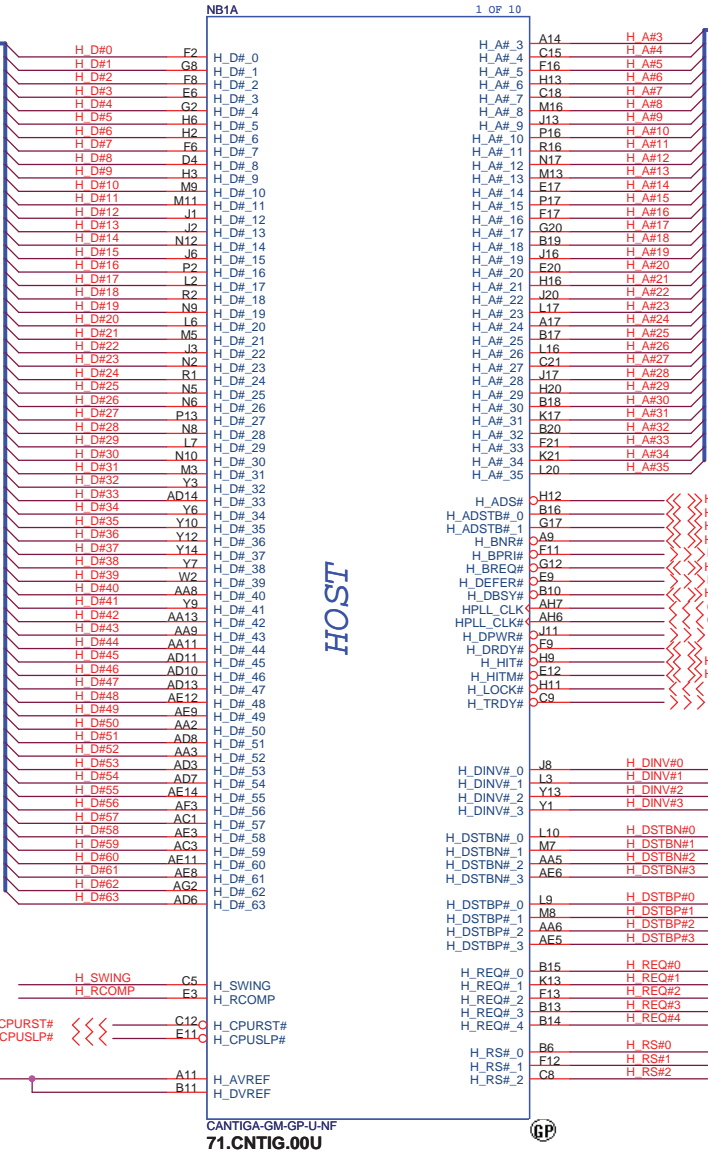
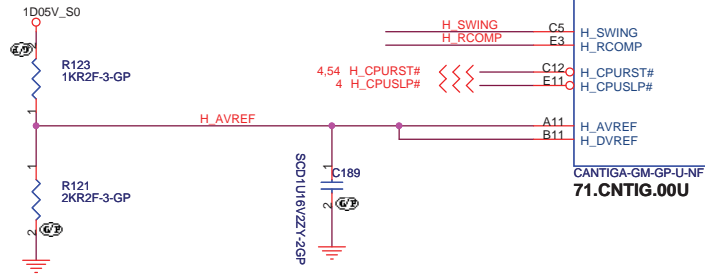
NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.







Place them near to the chip (< 0.5")



HOST

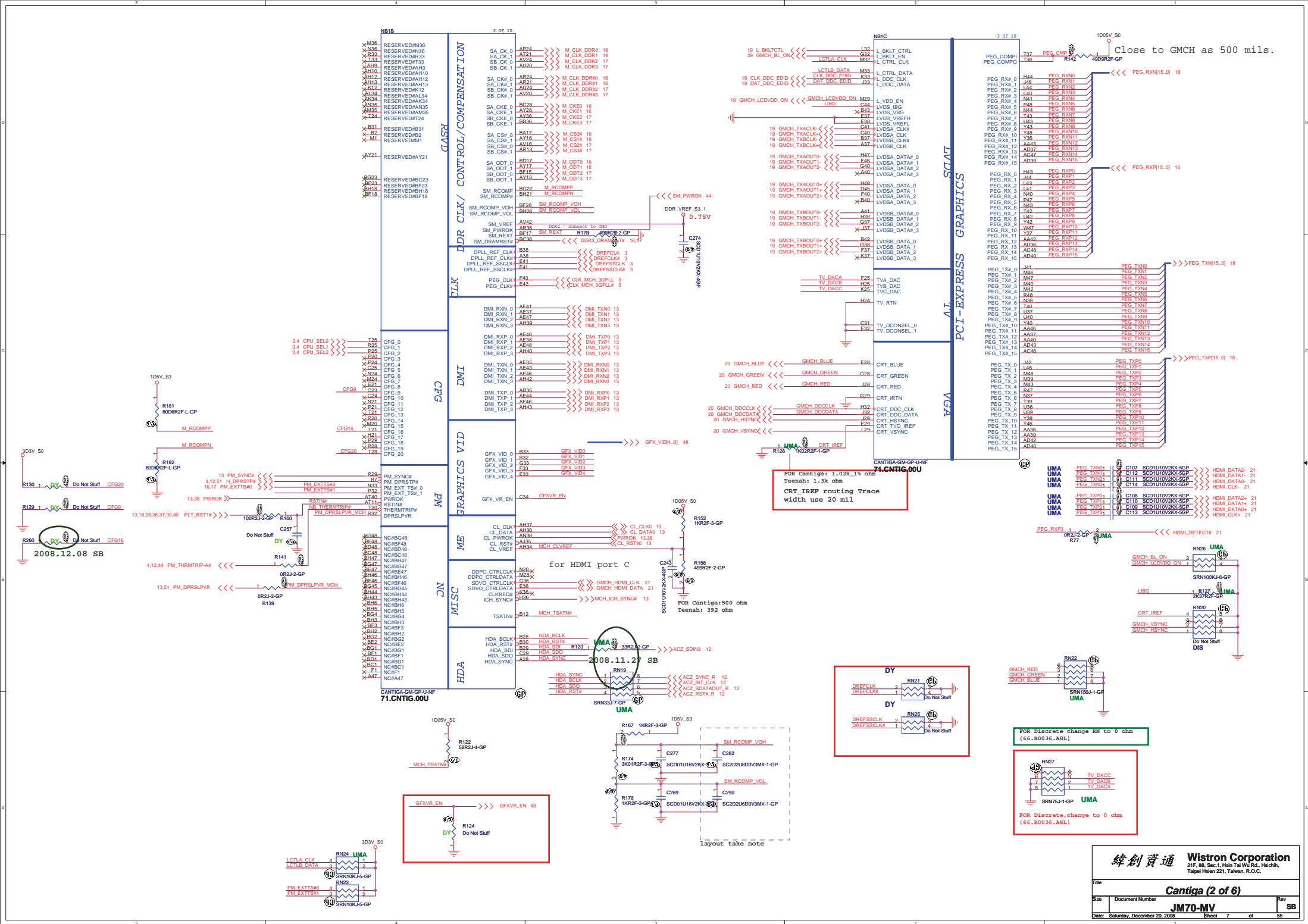
UMA

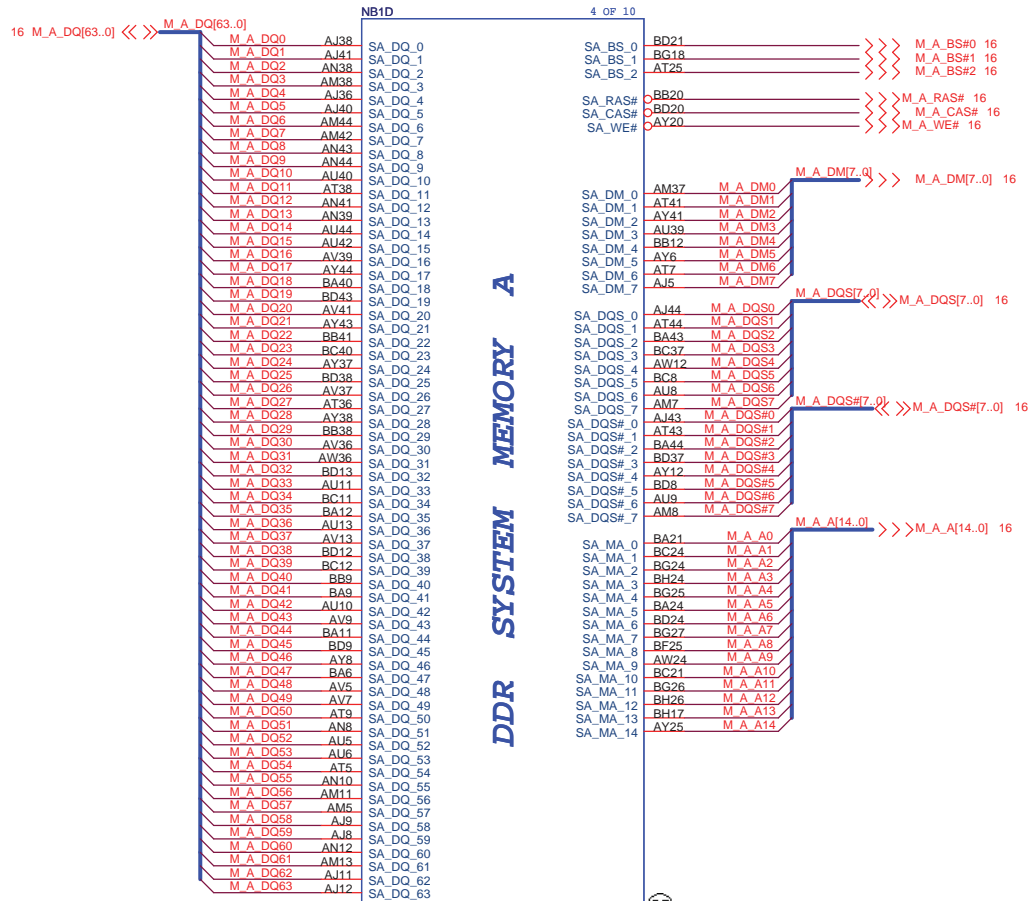
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cantiga (1 of 6)**

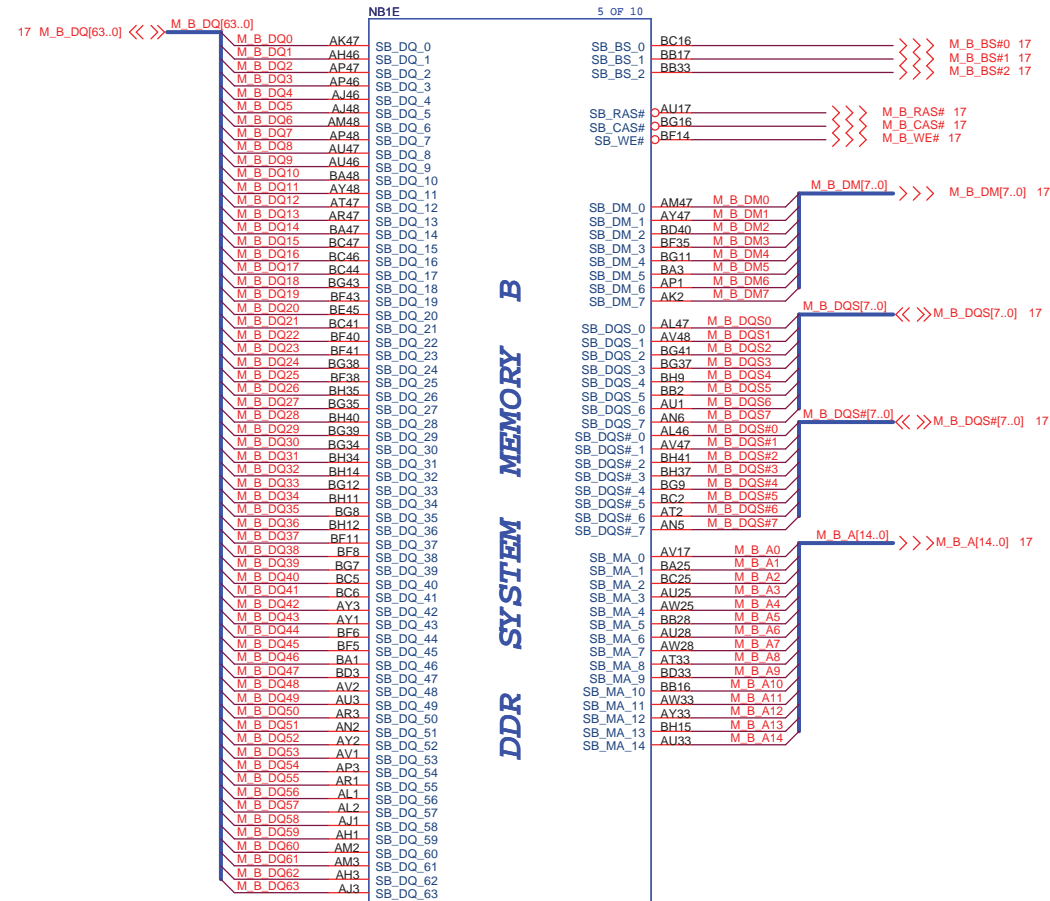
Size: Document Number: **JM70-MV** Rev: **SB**

Date: Saturday, December 20, 2008 Sheet 6 of 55





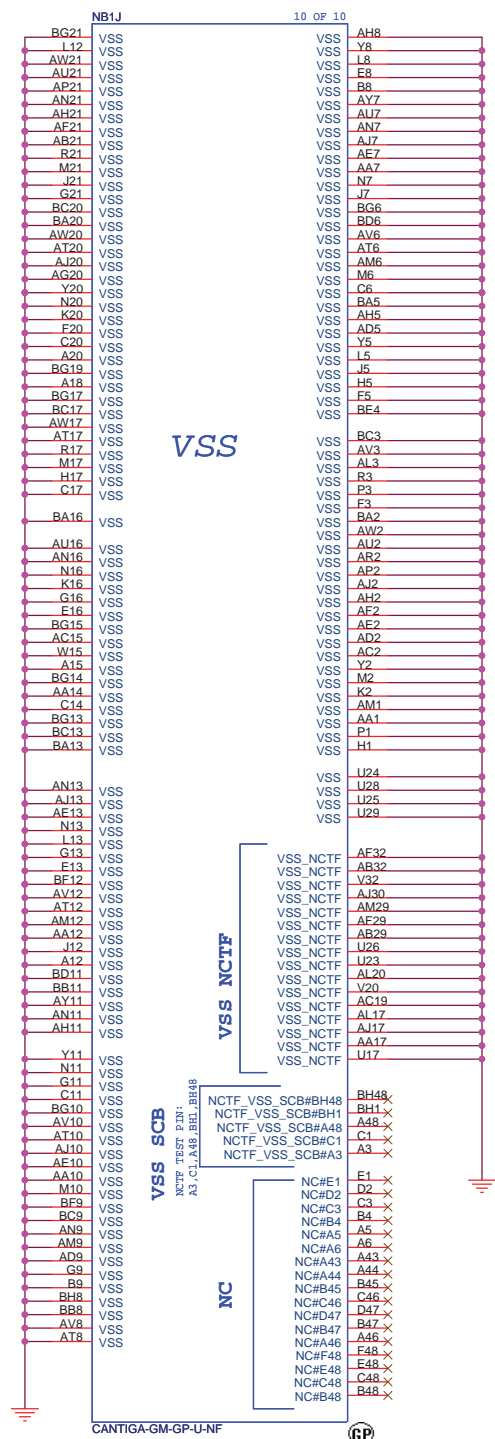
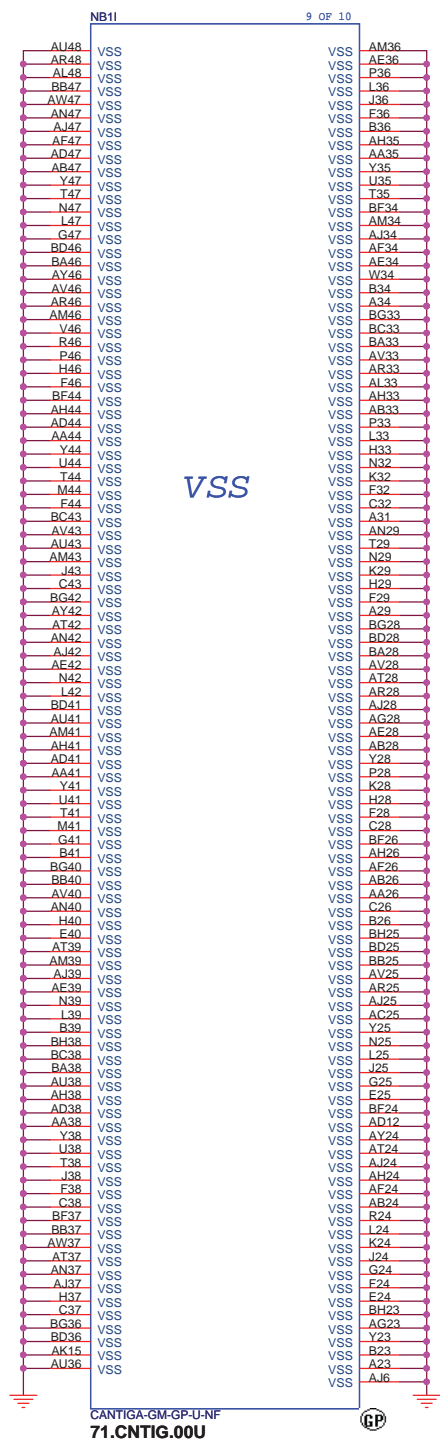
CANTIGA-GM-GP-U-NF
71.CNTIG.00U



CANTIGA-GM-GP-U-NF
71.CNTIG.00U

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Cantiga (3 of 6)			
Size	Document Number		Rev
	JM70-MV		SE
Date:	Saturday, December 20, 2008		Sheet 8 of 55



緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cantiga (6 of 6)

Size

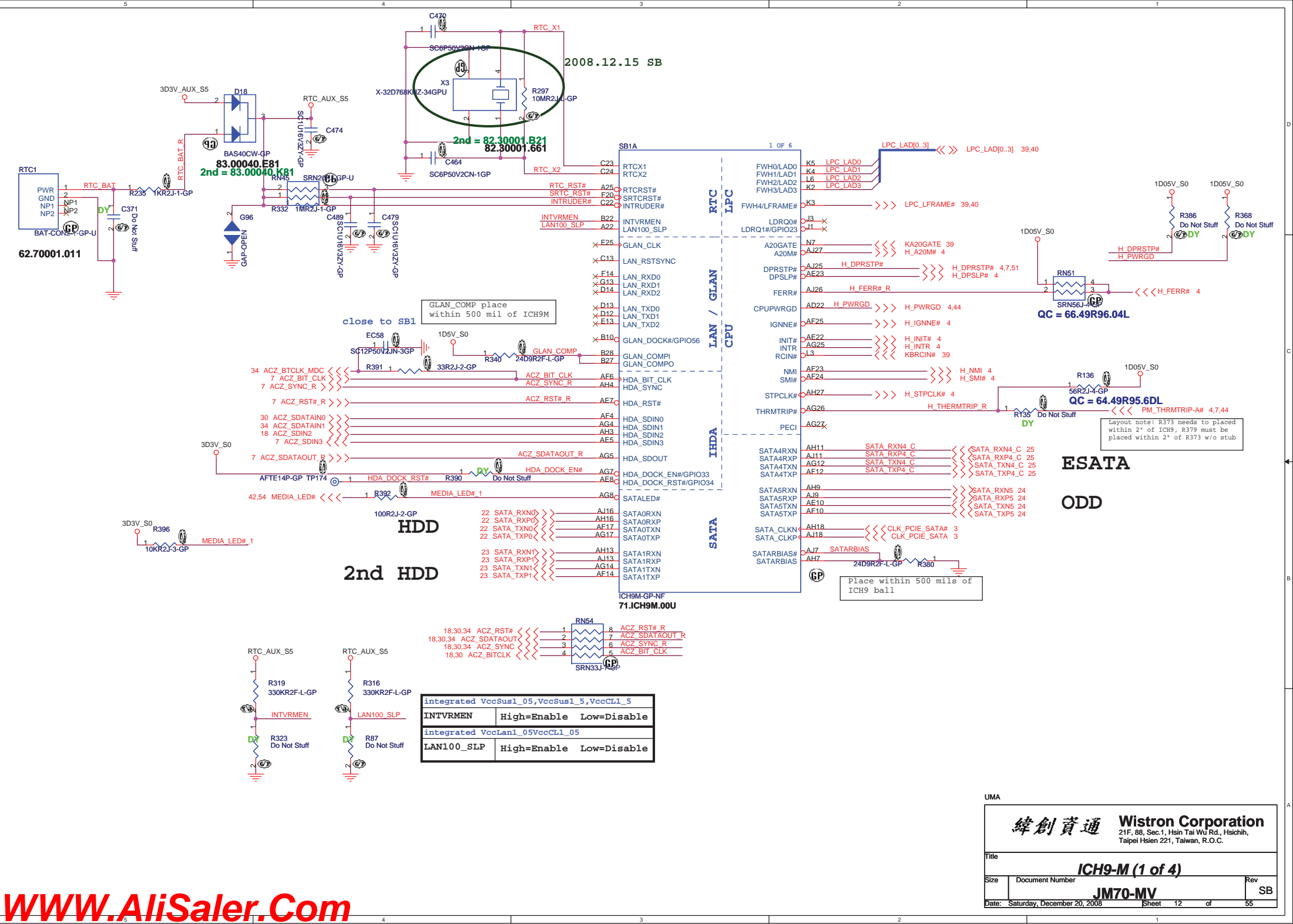
Document Number

Rev

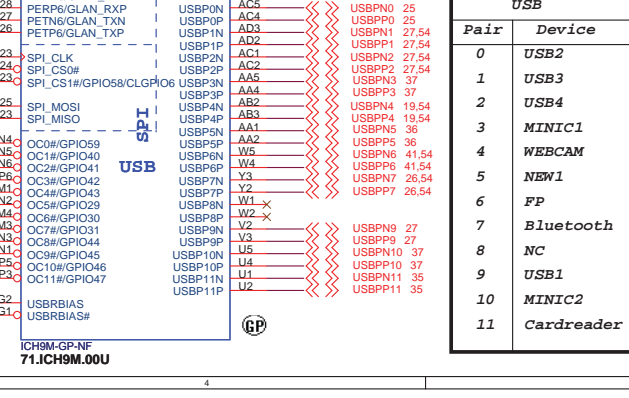
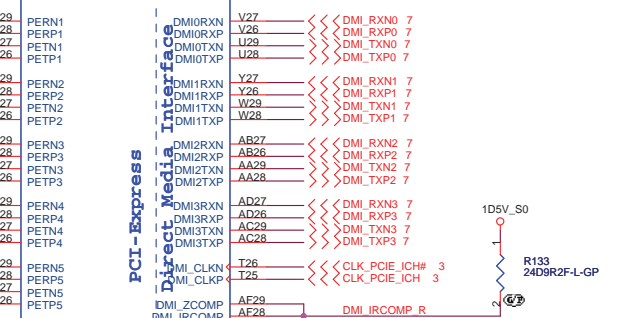
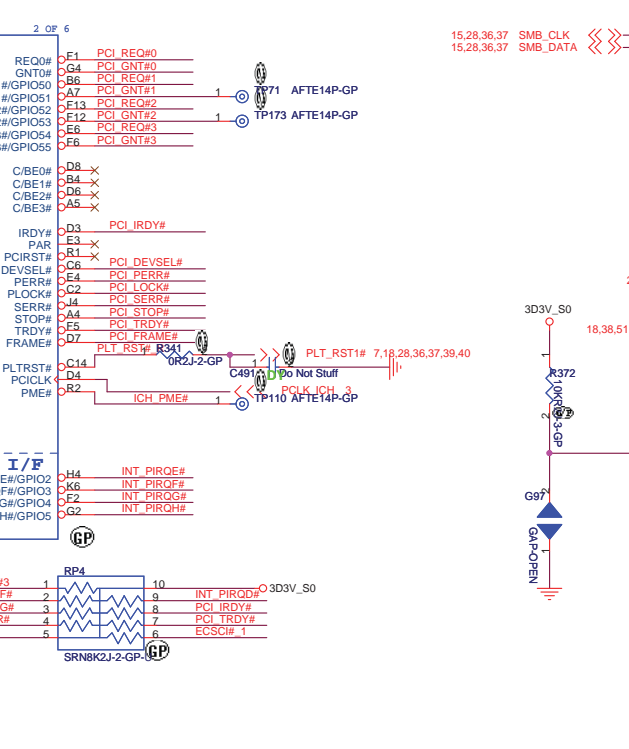
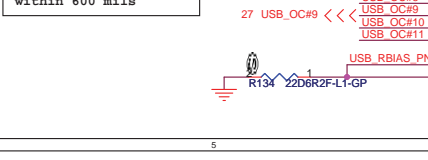
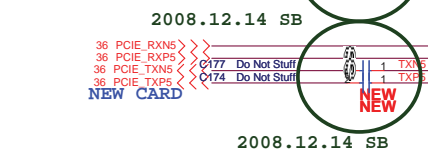
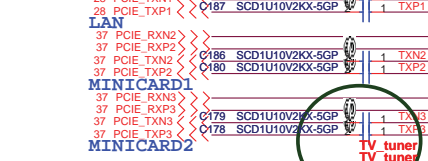
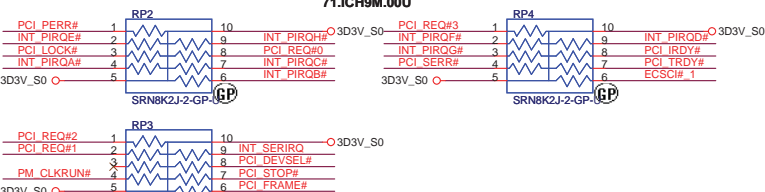
SB

Date: Saturday, December 20, 2008

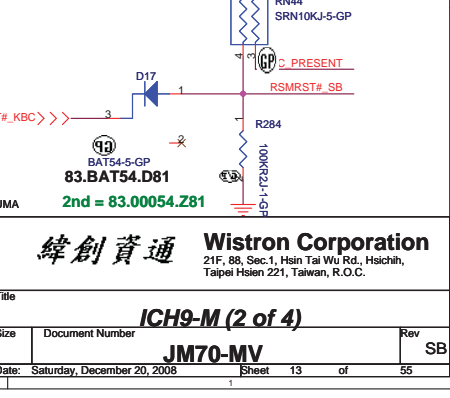
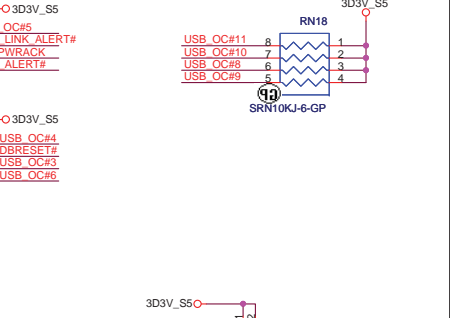
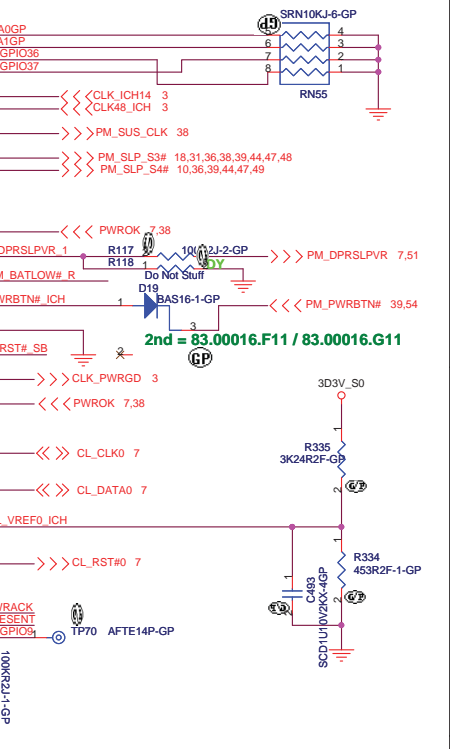
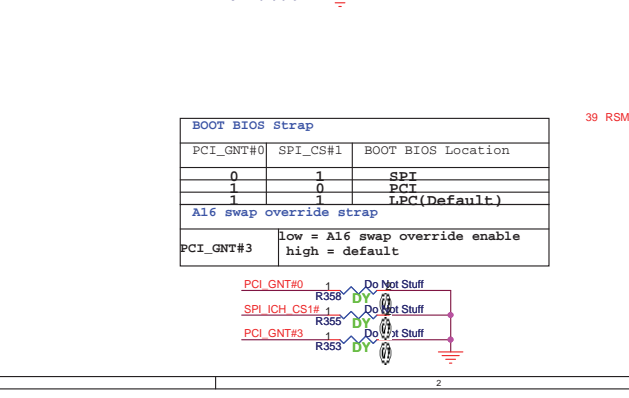
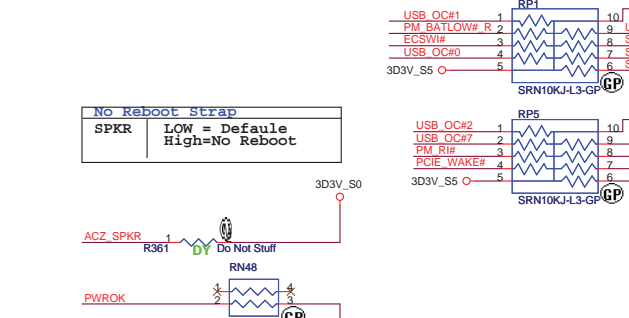
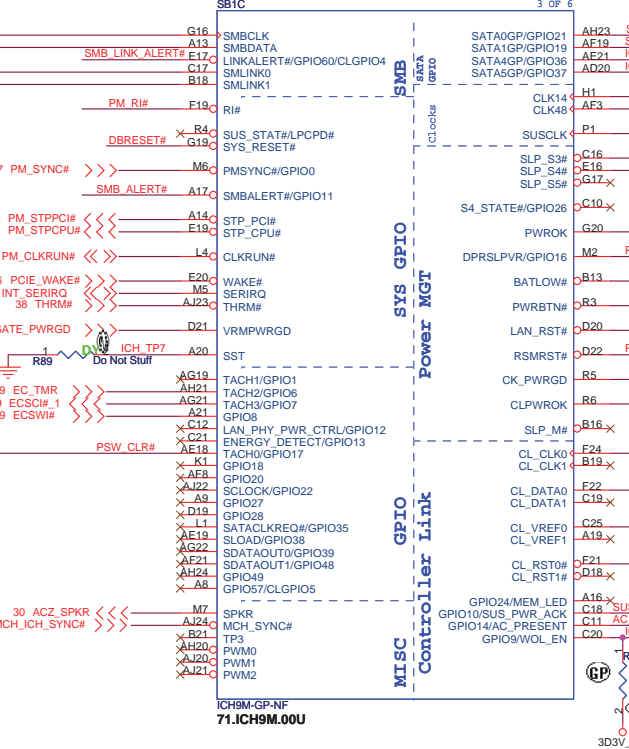
Sheet 11 of 55



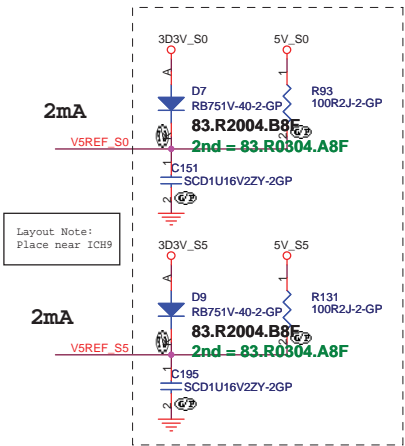
PCI_GNT#0 and SPI_CS1#
have weak internal Pull up



USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINIC1
4	WEBCAM
5	NEW1
6	FP
7	Bluetooth
8	NC
9	USB1
10	MINIC2
11	Cardreader

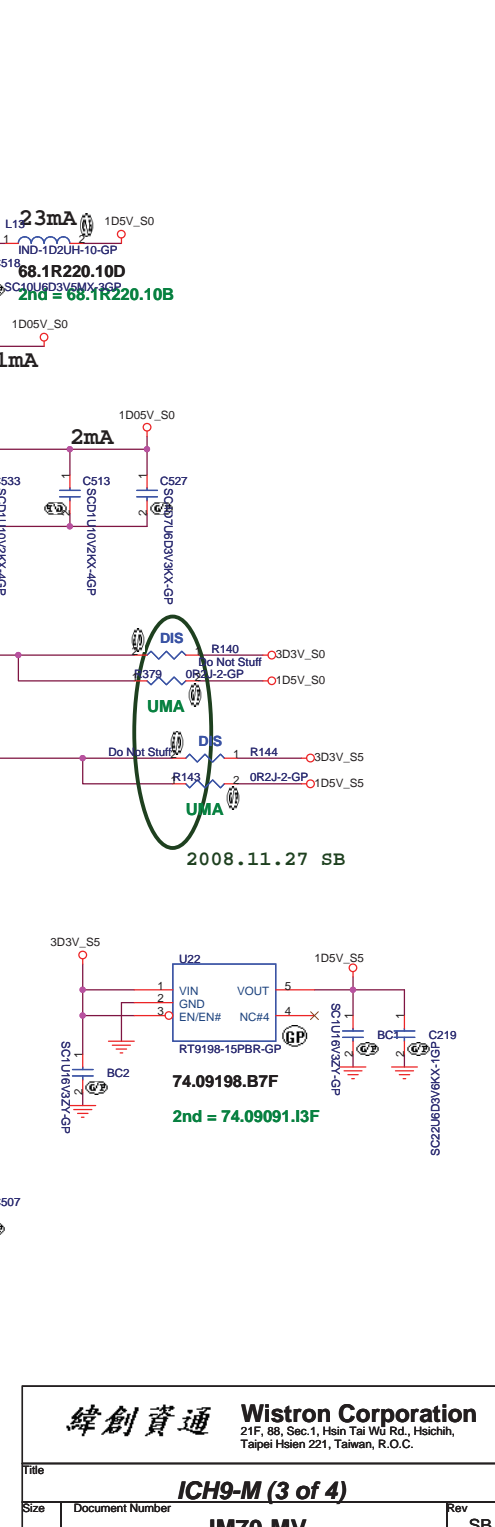
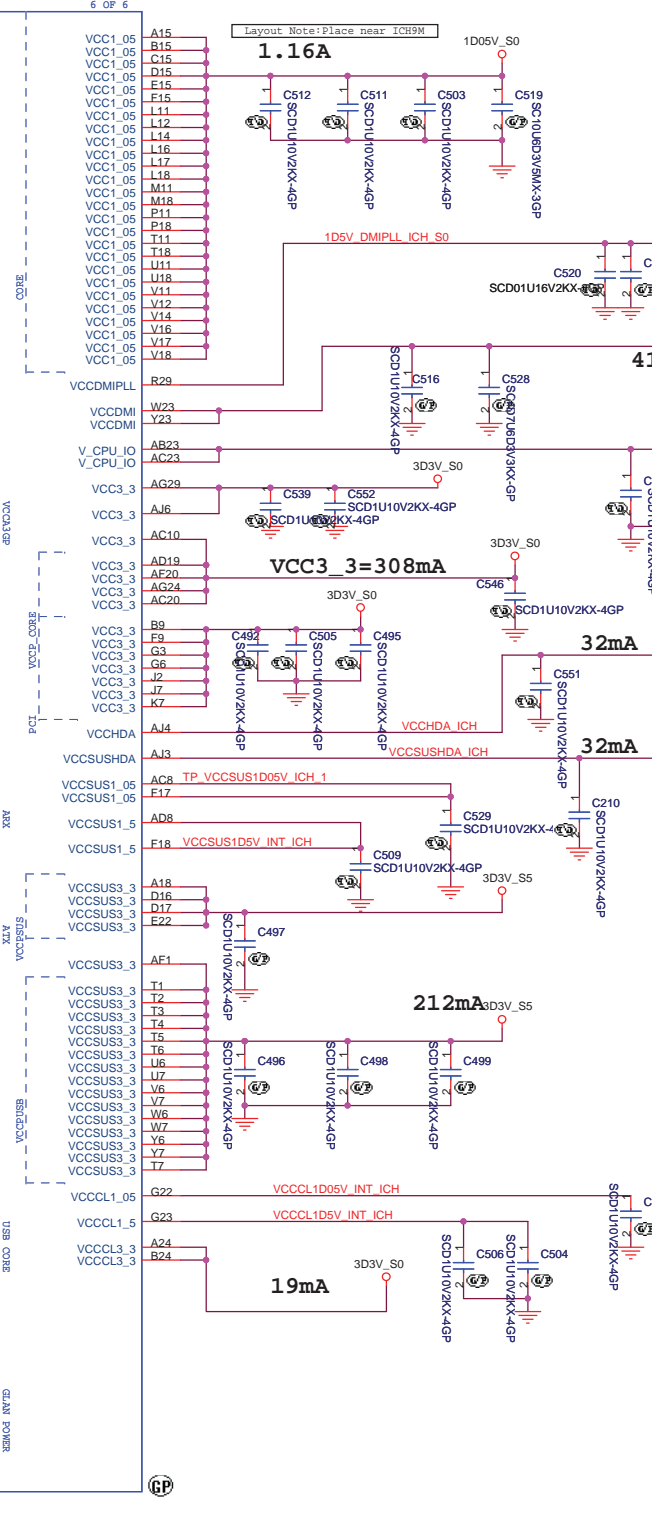
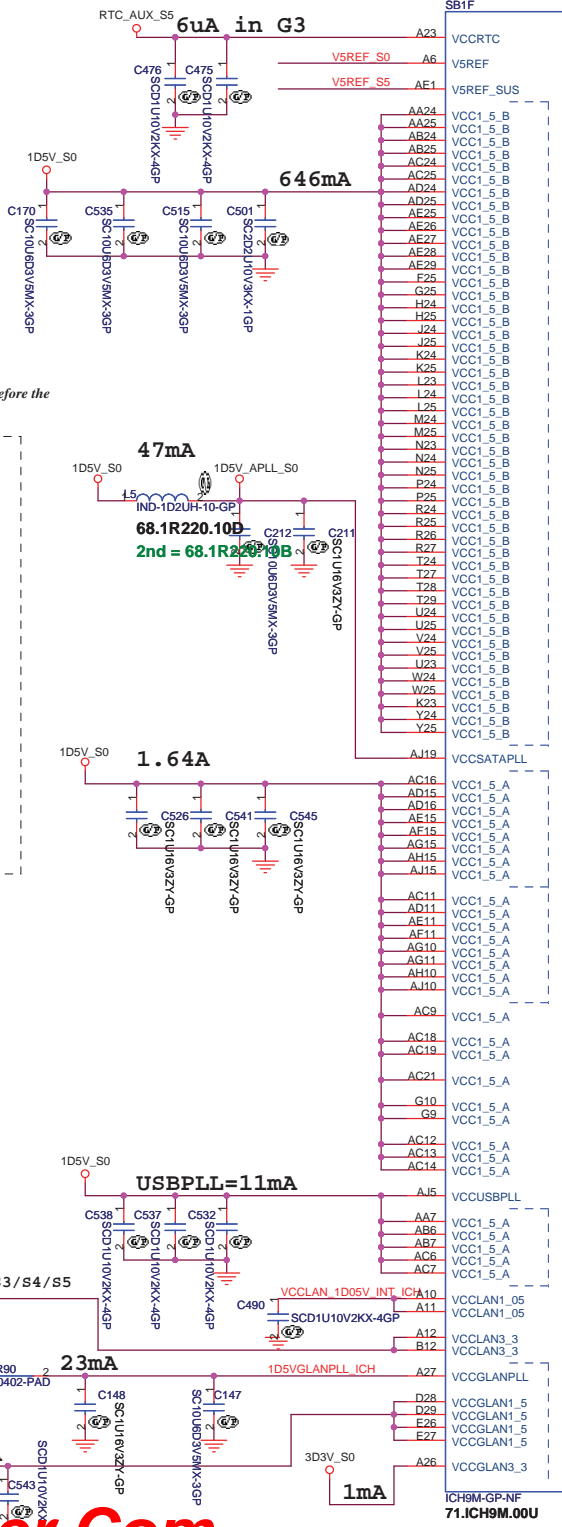


*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail



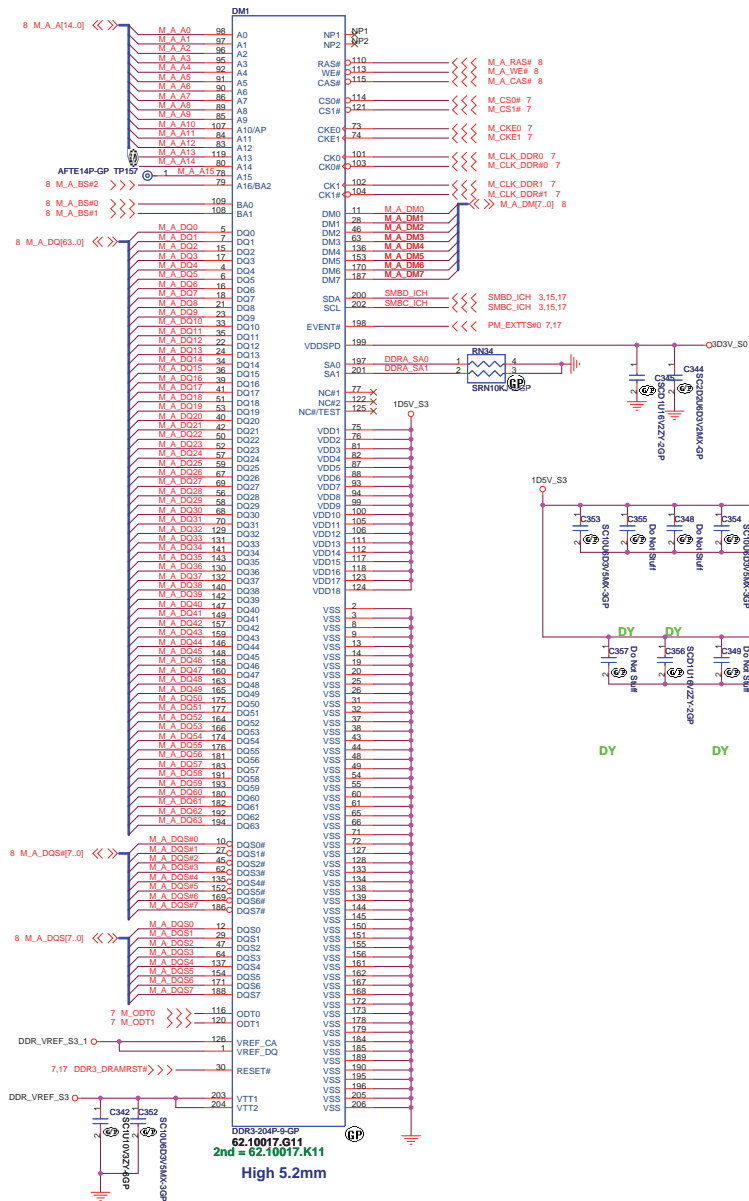
Layout Note:
Place near ICH9

WWW.AliSaler.Com

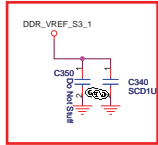




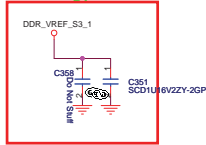
DDR3 SOCKET 1



Layout Note : Near Pin 126

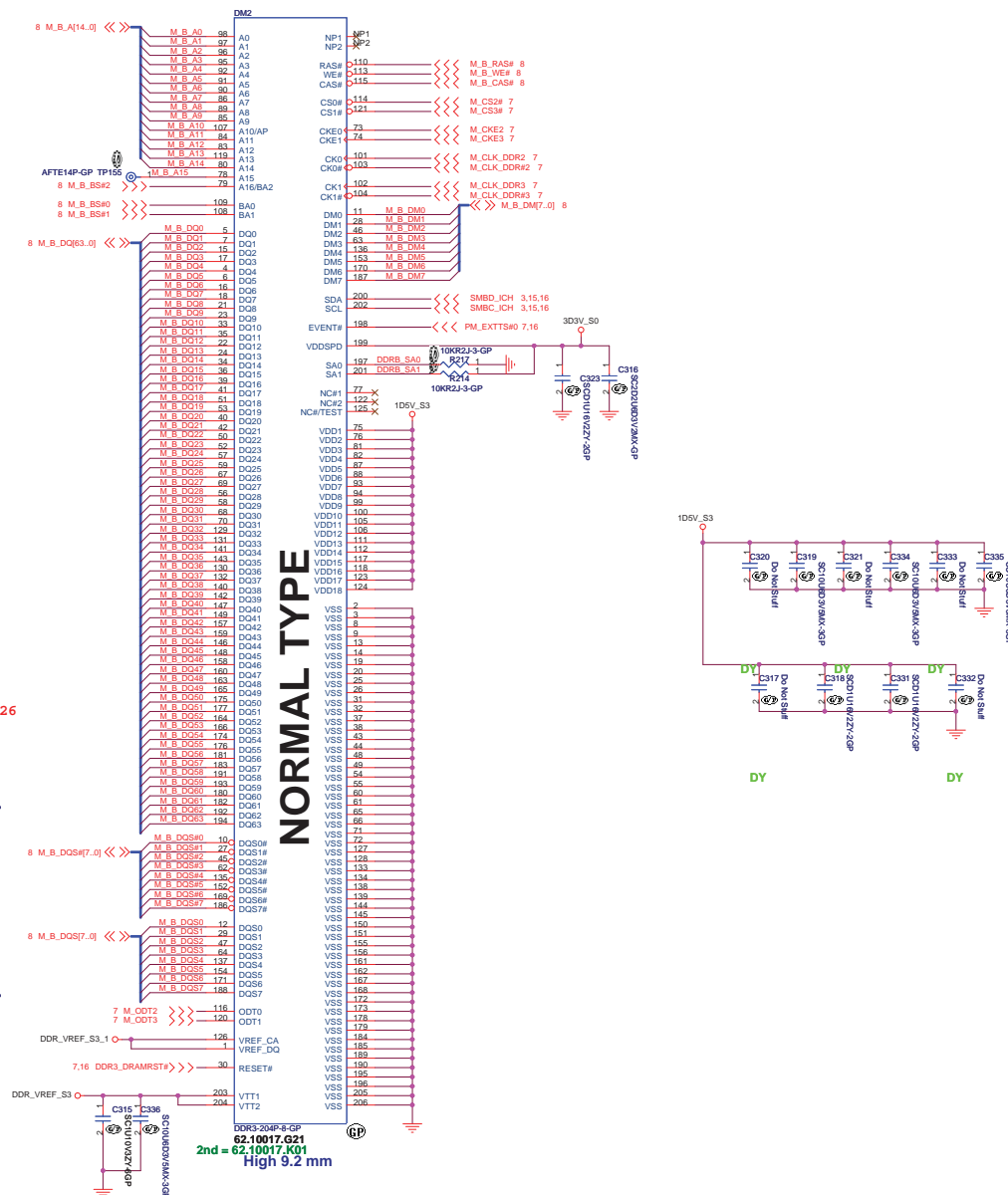


Layout Note: Near Pin 1

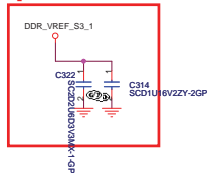


DY

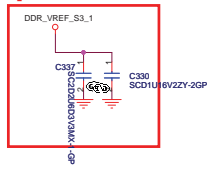
DDR3 SOCKET_2



Layout Note : Near Pin 126

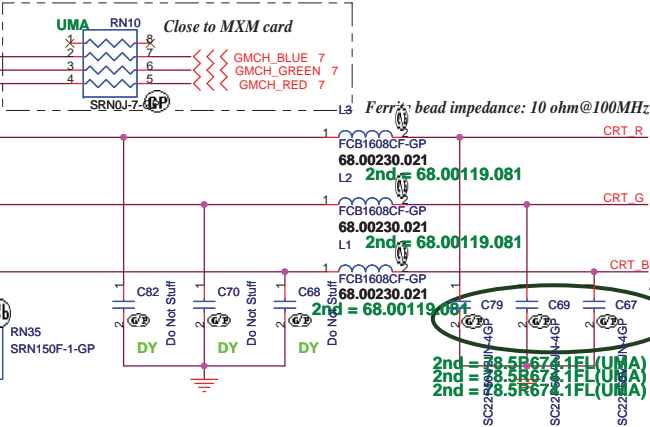


Layout Note : Near Pin 1

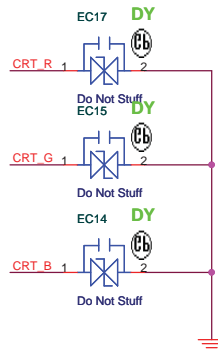


NORMAL TYPE

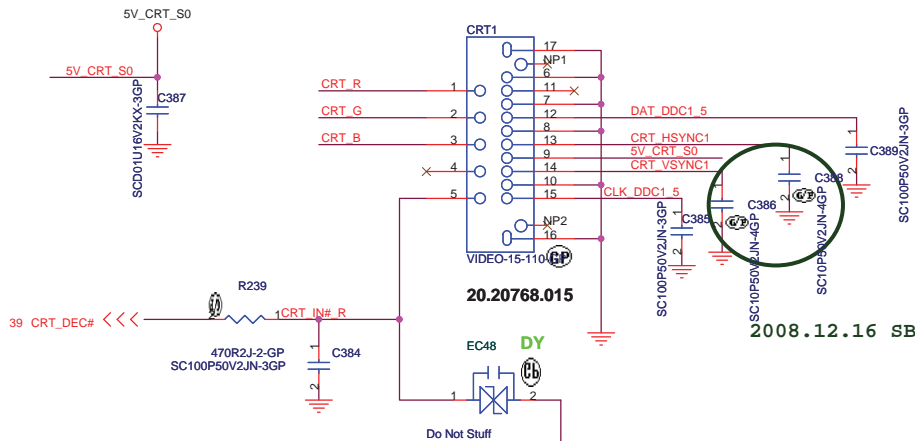
Layout Note:
Place these resistors
close to the CRT-out
connector



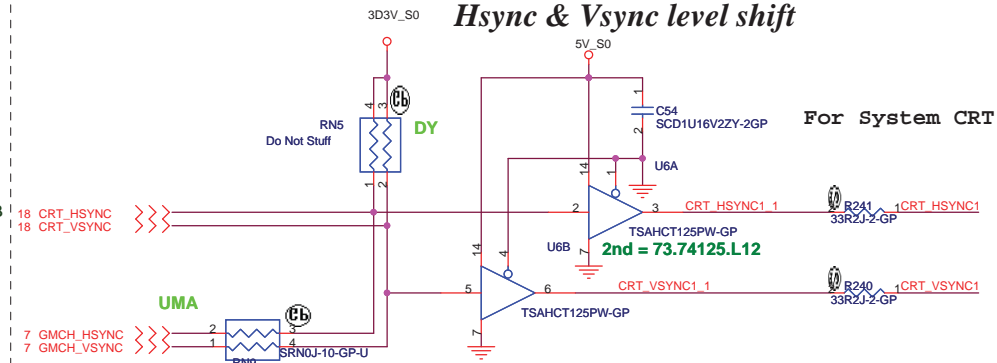
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



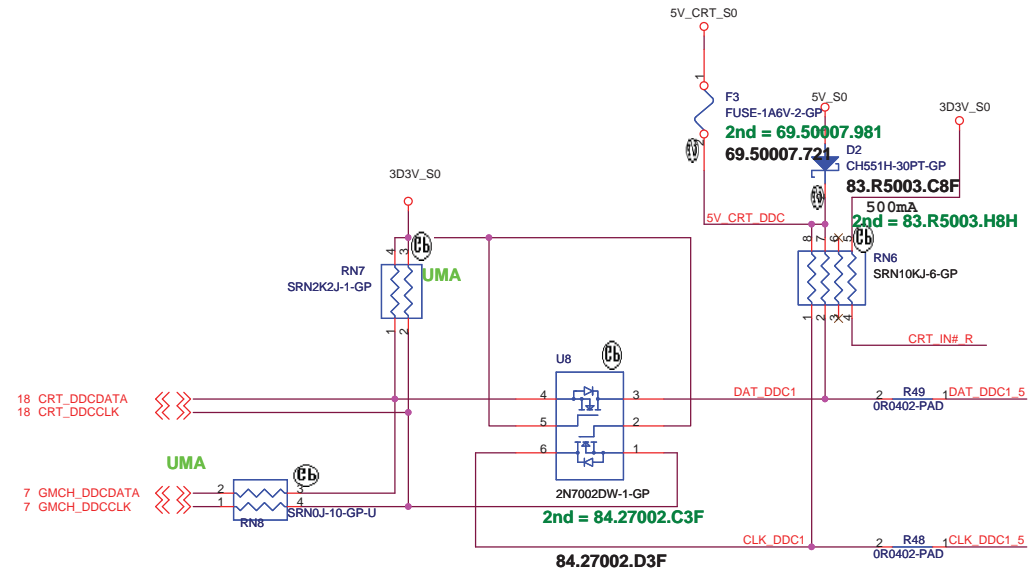
CRT I/F & CONNECTOR



Hsync & Vsync level shift



DDC_CLK & DATA level shift

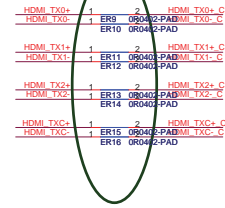
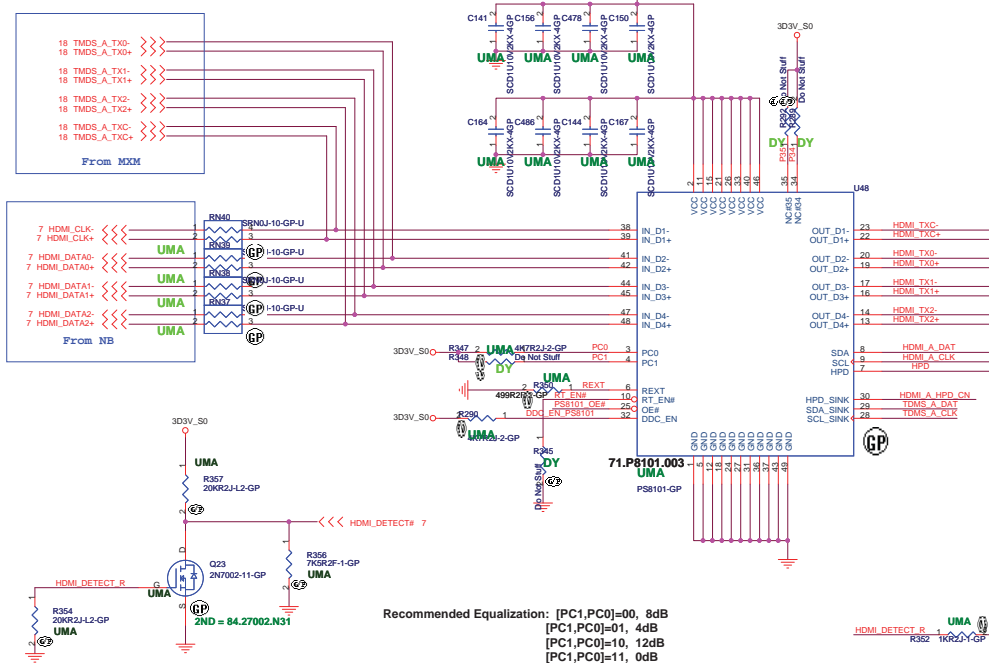
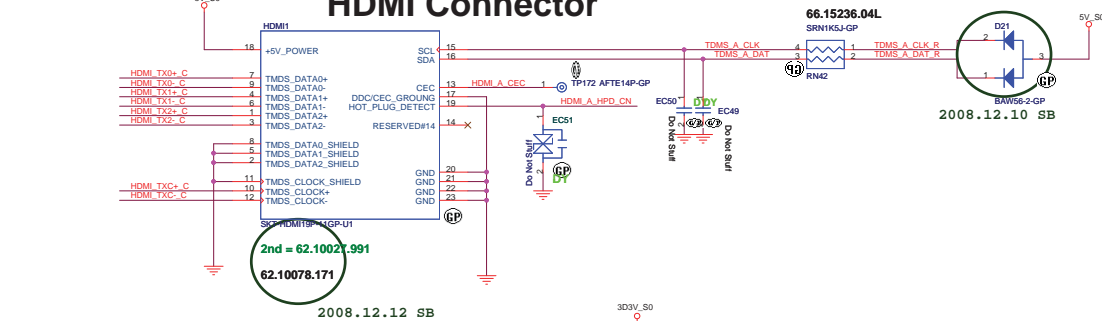


UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		CRT CONN	
Size	Document Number	Rev	
		JM70-MV	
Date:	Saturday, December 20, 2008	Sheet	20 of 55

HDMI Connector



2008.12.14 SB



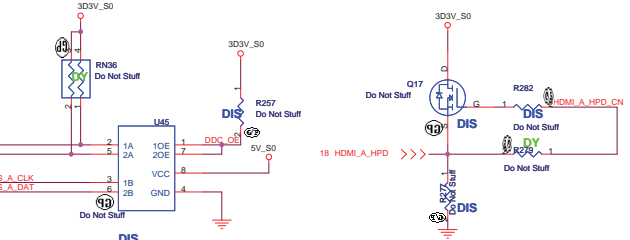
2008.12.14 SB



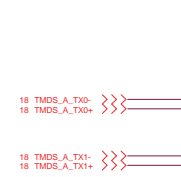
2008.12.14 SB



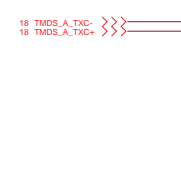
2008.12.14 SB



2008.12.14 SB



2008.12.14 SB



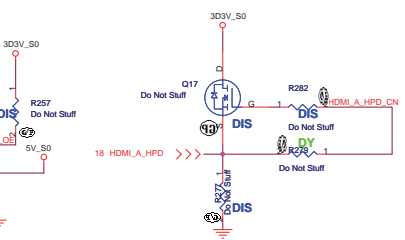
2008.12.14 SB



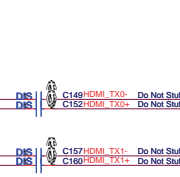
2008.12.14 SB



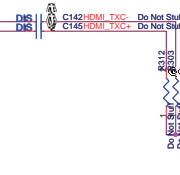
2008.12.14 SB



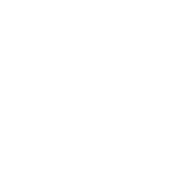
2008.12.14 SB



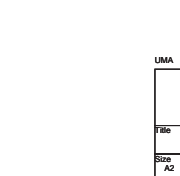
2008.12.14 SB



2008.12.14 SB

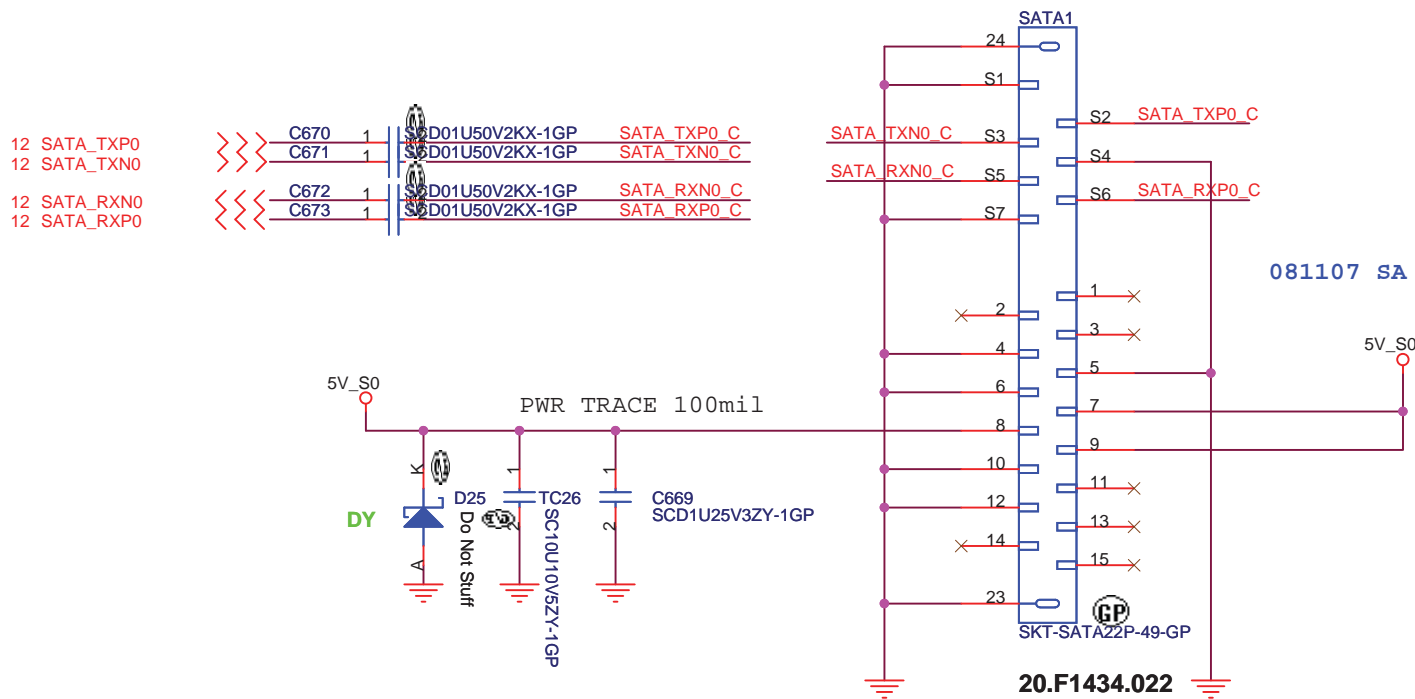


2008.12.14 SB



2008.12.14 SB

SATA Connector



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

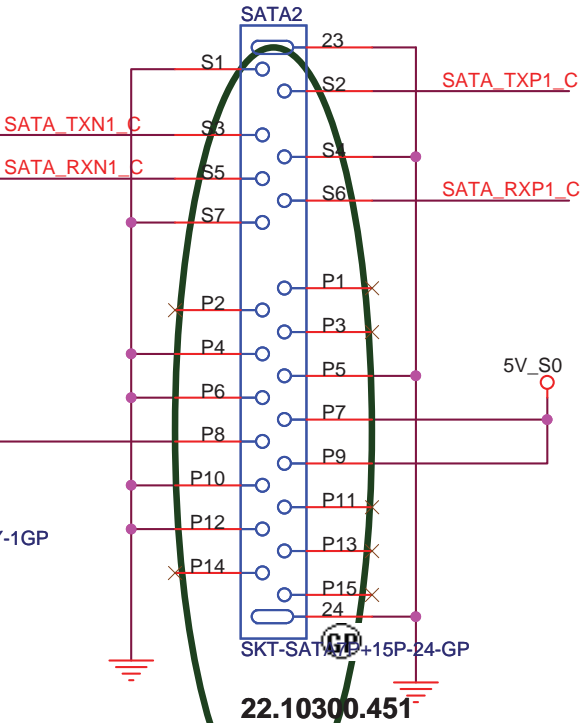
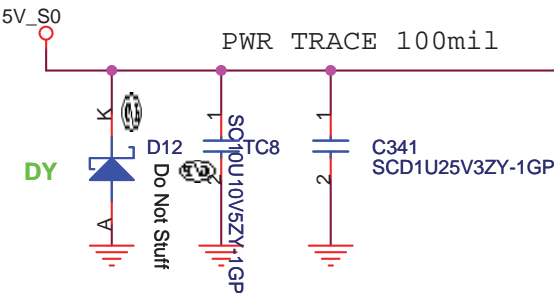
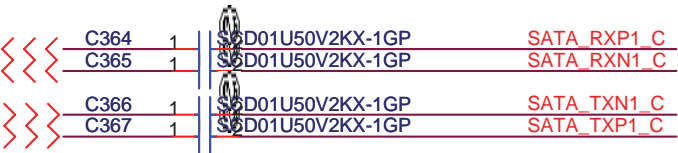
Title				
HDD CONN				
Size	Document Number			Rev
	JM70-MV			SB
Date: Saturday, December 20, 2008		Sheet	22	of 55

2nd HDD SATA Connector

2008.12.12 SB

12 SATA_RXP1
12 SATA_RXN1

12 SATA_TXN1
12 SATA_TXP1



UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

2nd HDD

Size

Document Number

JM70-MV

Rev

SB

Date: Saturday, December 20, 2008

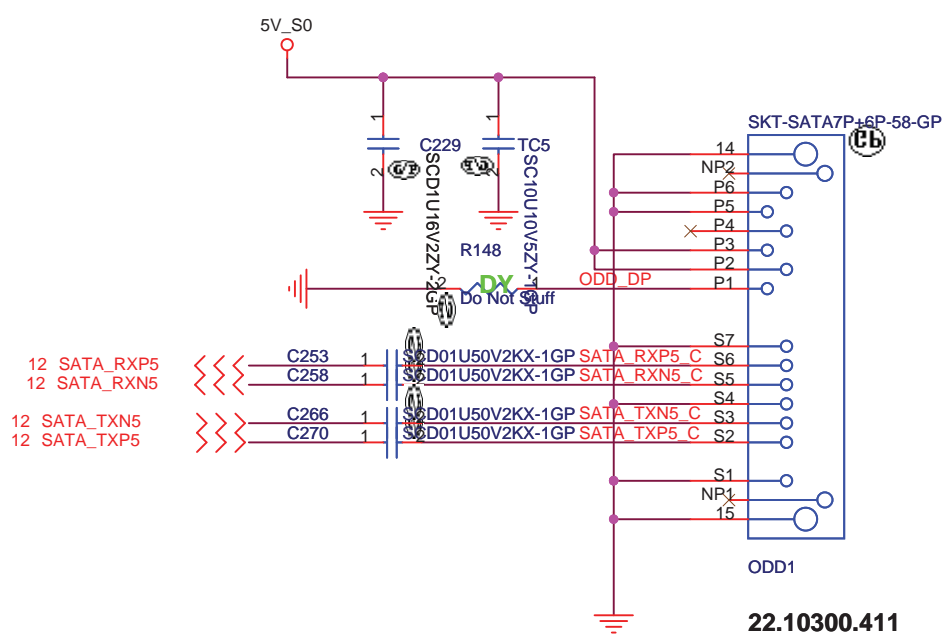
Sheet

23

of

55

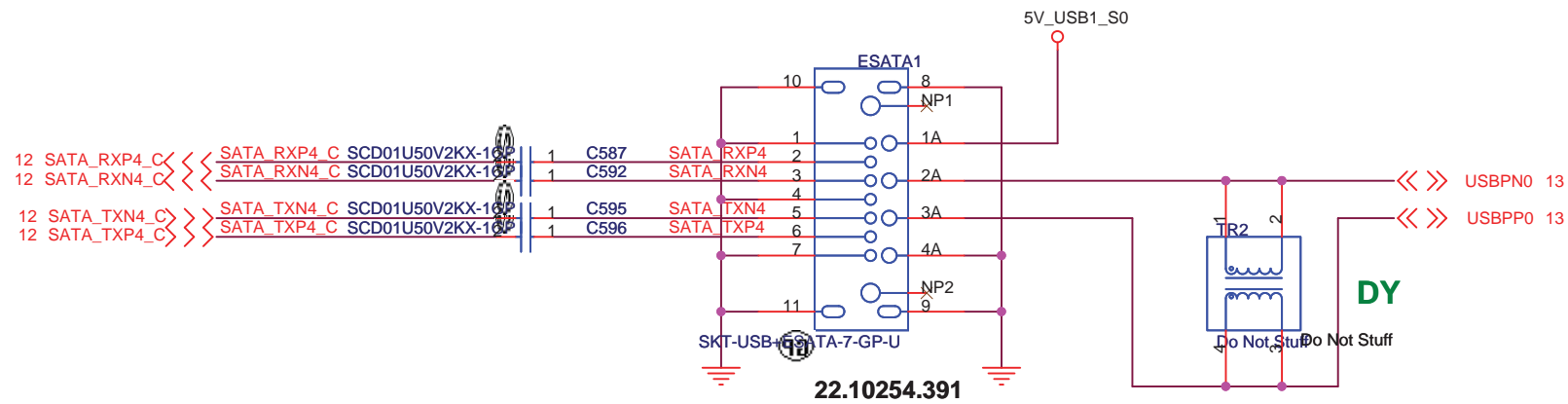
ODD Connector



UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
ODD			
Size	Document Number		Rev
	JM70-MV		SB
Date: Saturday, December 20, 2008		Sheet 24 of 55	

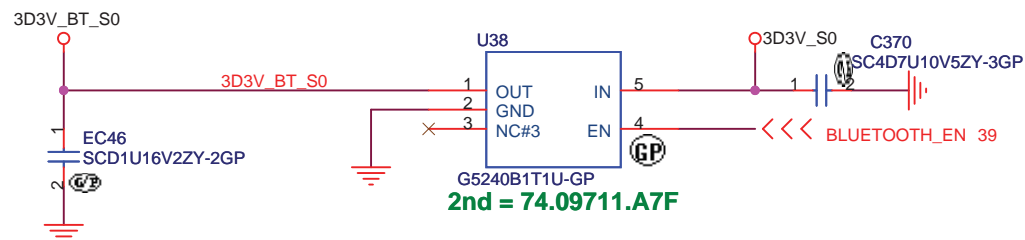
ESATA Connector



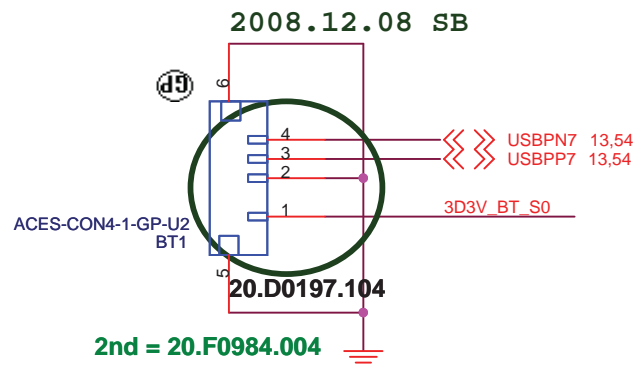
UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title ESATA			
Size A4	Document Number JM70-MV		Rev SB
Date: Saturday, December 20, 2008	Sheet 25	of 55	

BLUETOOTH MODULE



EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BLUETOOTH

Size

Document Number

JM70-MV

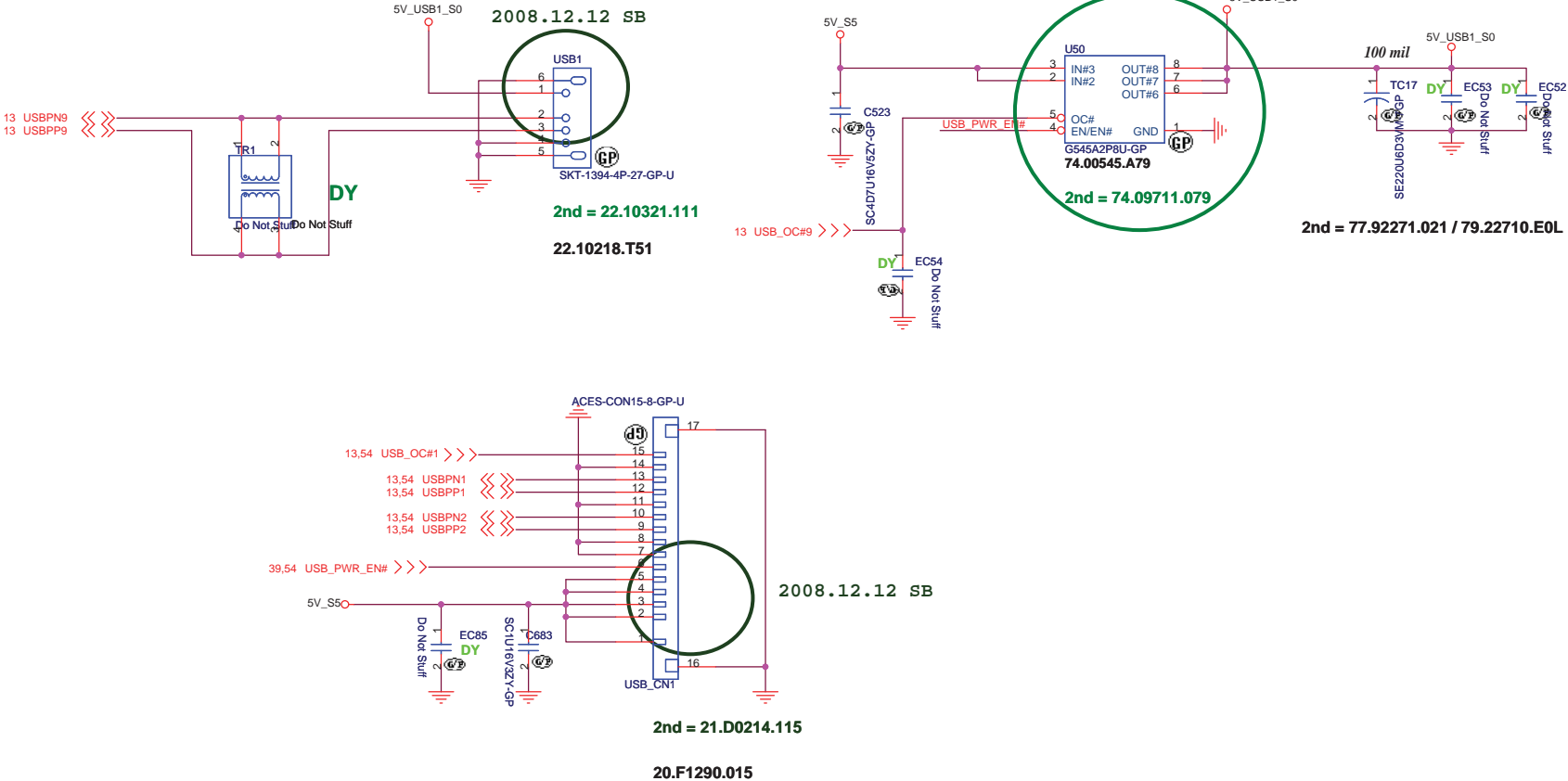
Rev

SB

Date: Saturday, December 20, 2008

Sheet 26 of 55

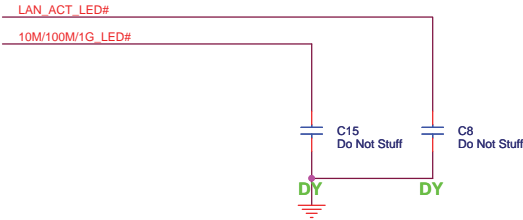
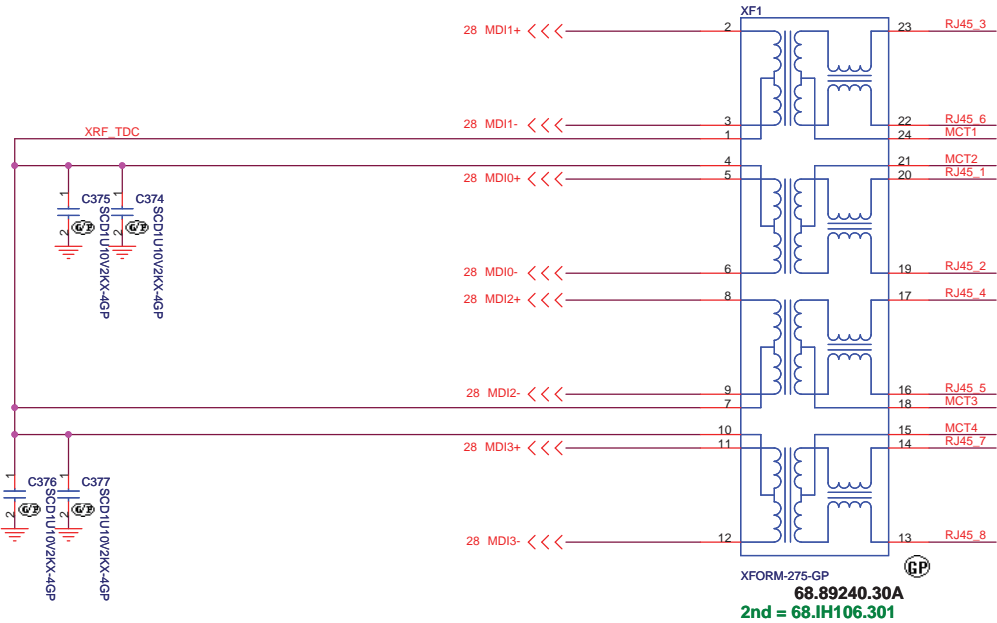
USB1 Connector



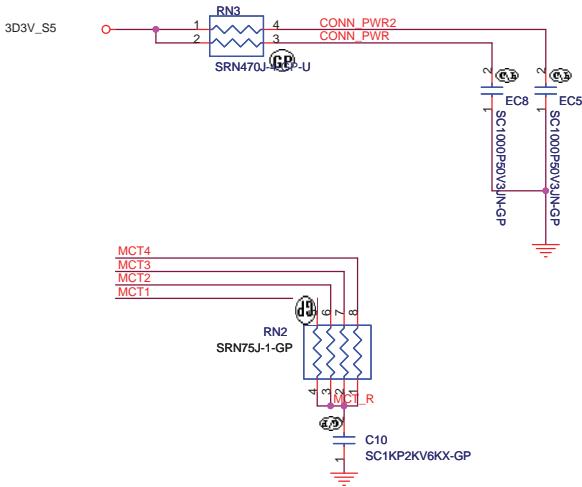
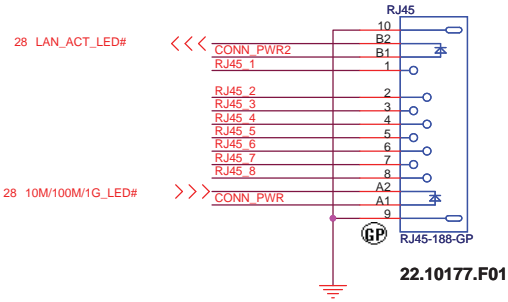
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

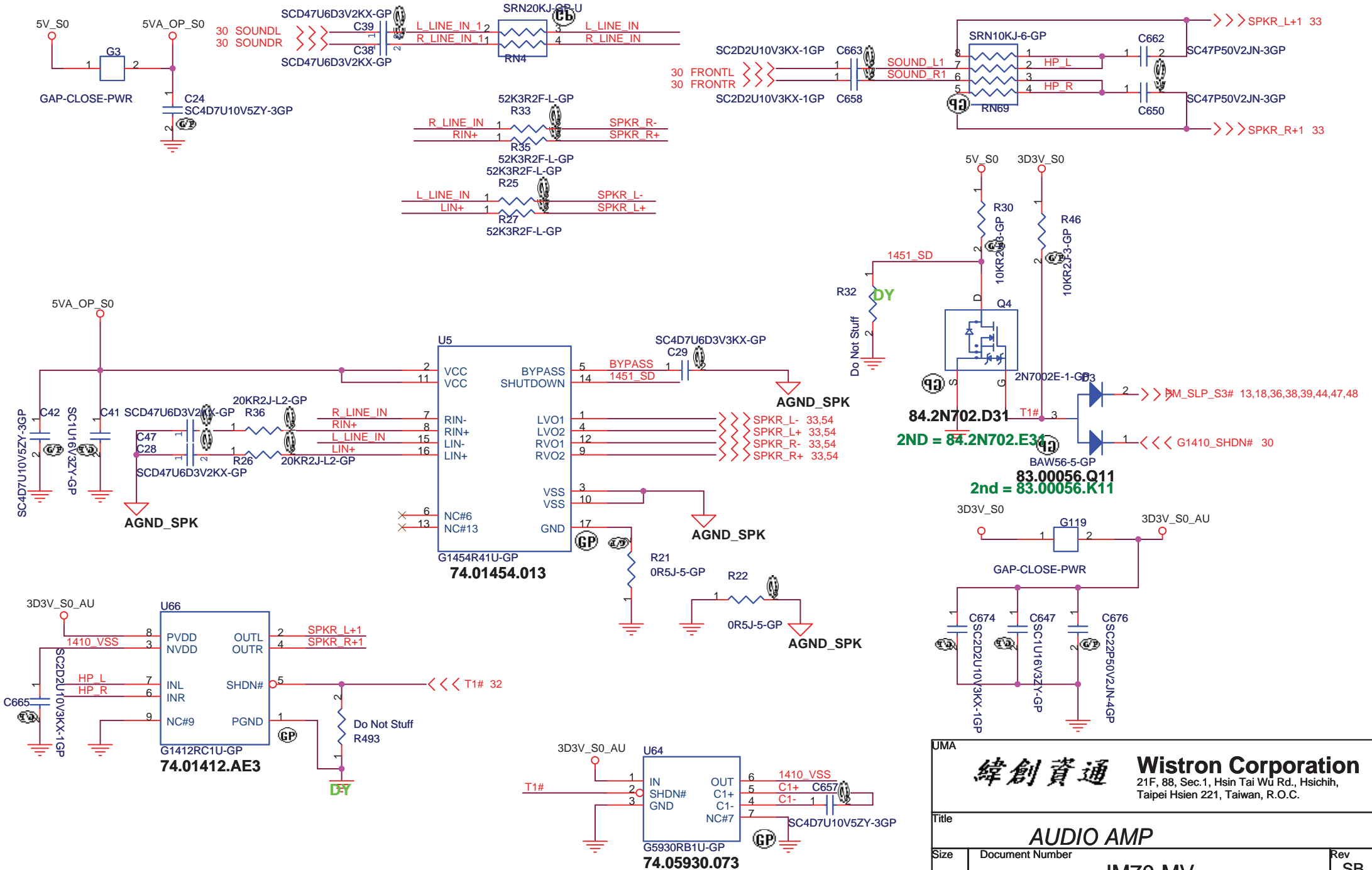
GIGA Lan Transformer

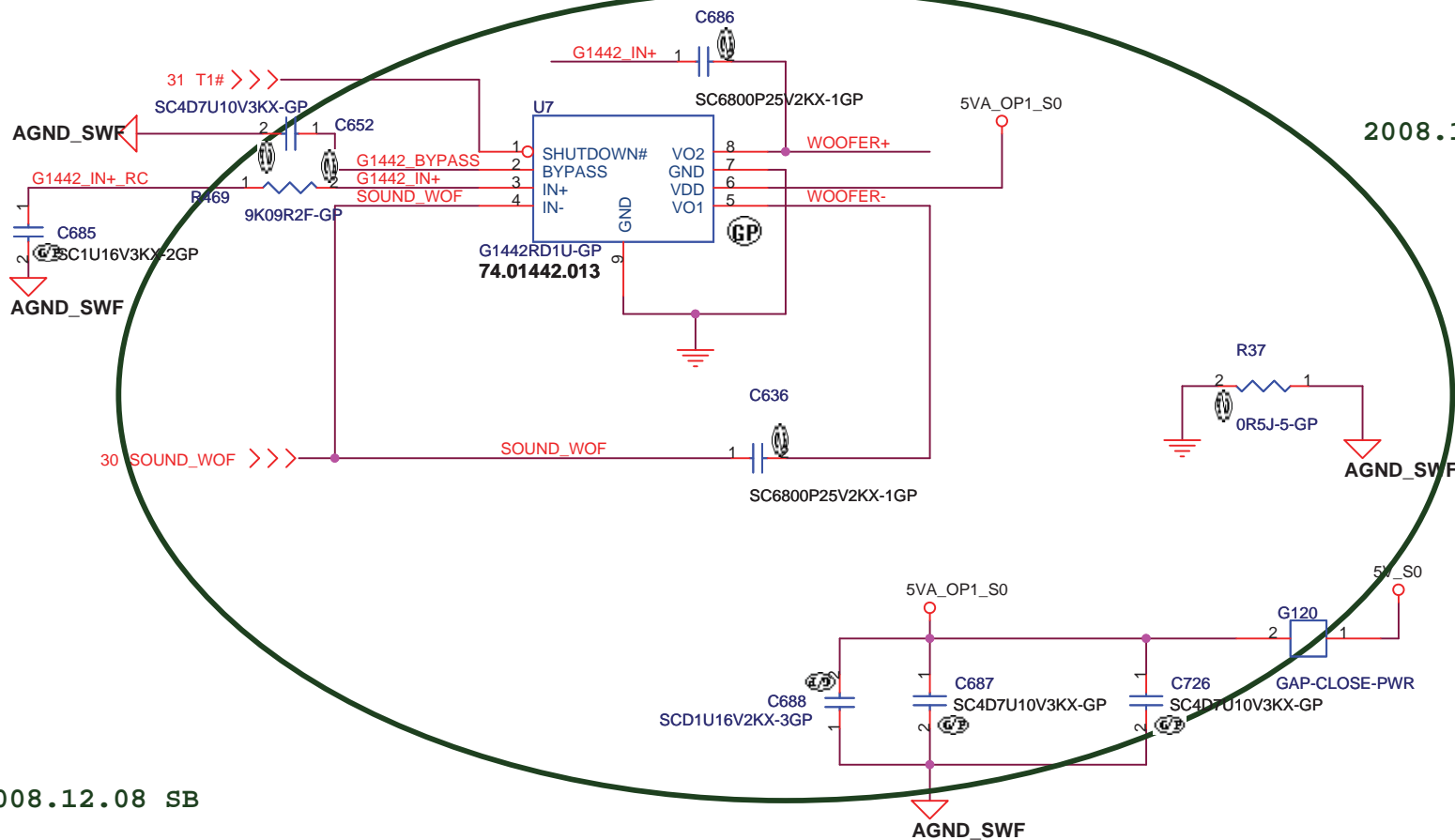


LAN Connector



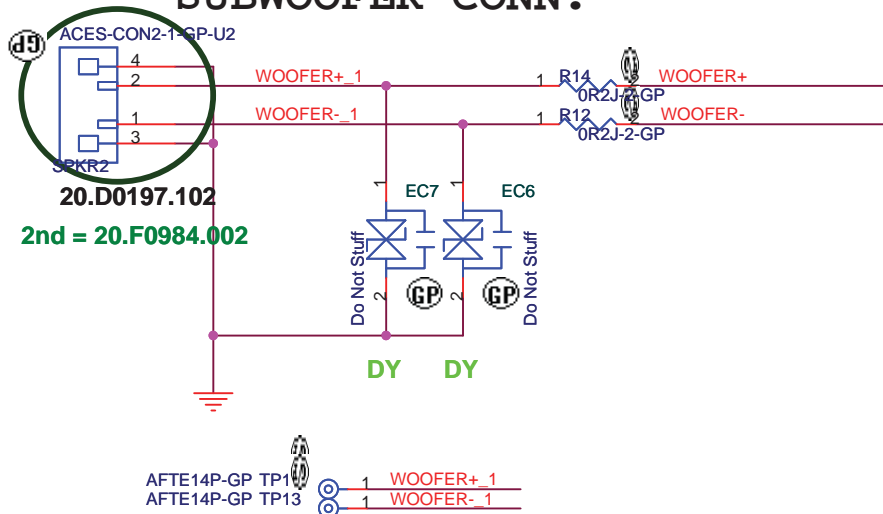
AUDIO OP AMPLIFIER





2008.12.08 SB

SUBWOOFER CONN.



AFTE14P-GP TP1
AFTE14P-GP TP13

UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SUBWOOFER CONN.

Size

Document Number

JM70-MV

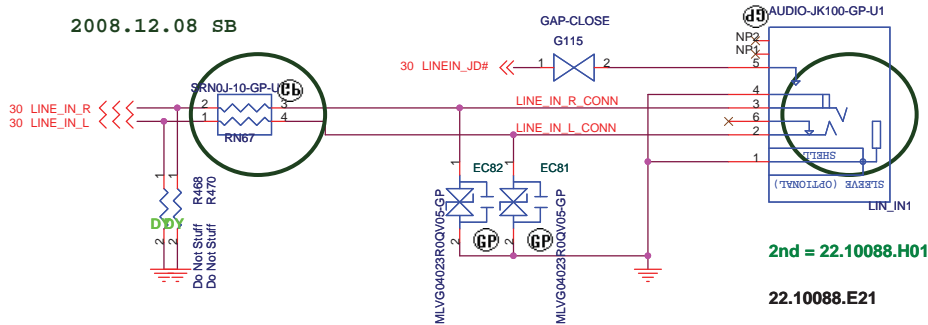
Rev
SB

Date: Saturday, December 20, 2008

Sheet 32 of 55

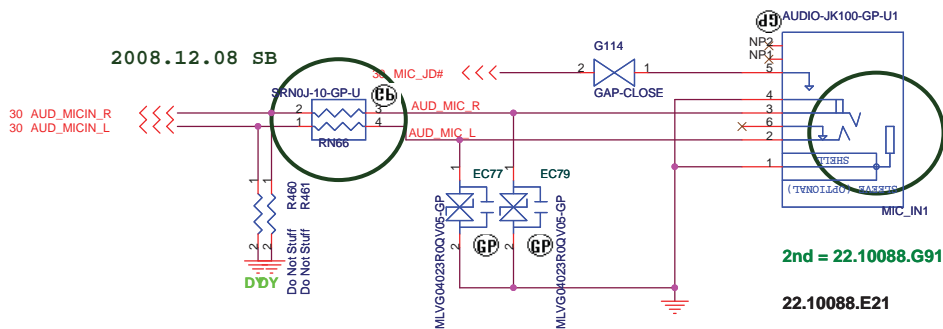
LINE IN

2008.12.08 SB



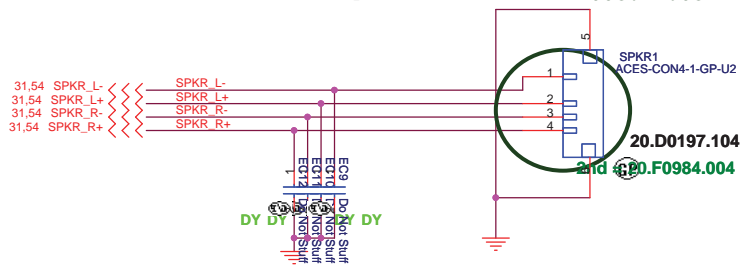
MIC IN

2008.12.08 SB



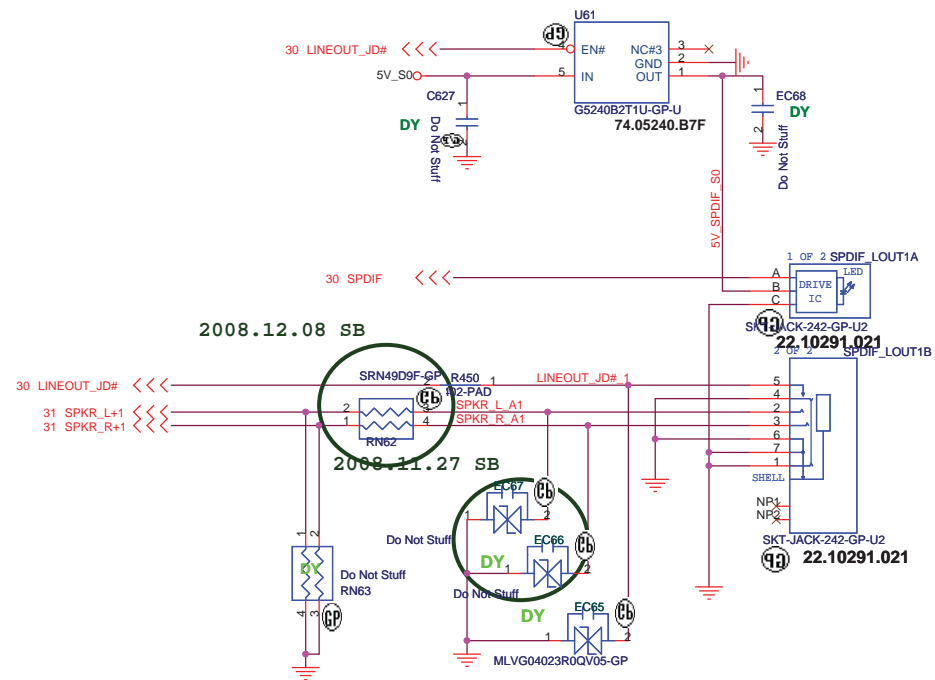
Internal Speaker

2008.12.08 SB



LINE OUT / SPDIF

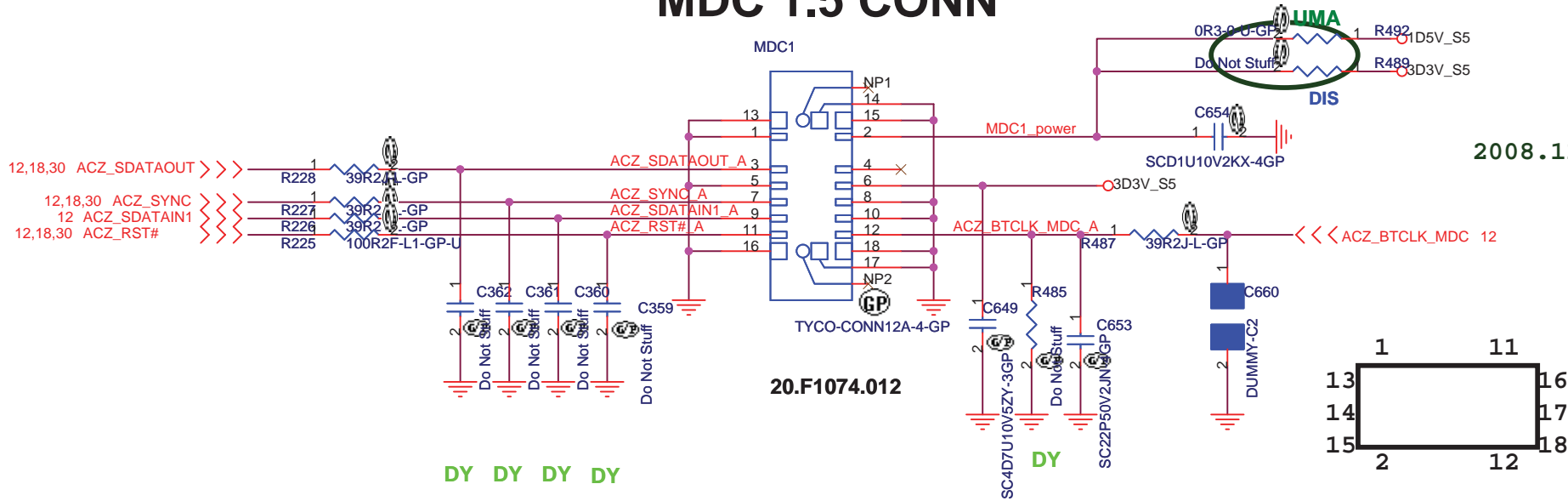
2008.12.08 SB



UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: AUDIO jack			
Size	Document Number	Rev	
	JM70-MV	SB	
Date: Saturday, December 20, 2008	Sheet 33	of 55	

MDC 1.5 CONN



2008.11.27 SB

A diagram of a rectangle with vertices labeled 1, 11, 16, 17, 18, 12, 2, 13, 14, 15. The labels are arranged as follows: 1 and 11 are at the top; 16 and 17 are on the right; 18, 12, and 2 are at the bottom; 13, 14, and 15 are on the left.

UMA

緯創資通

Wistron Corporation
815, 22, Sec. 1, Hsin-Tai W. Rd., Hsin-Tai

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

MDC

Size

Document Number

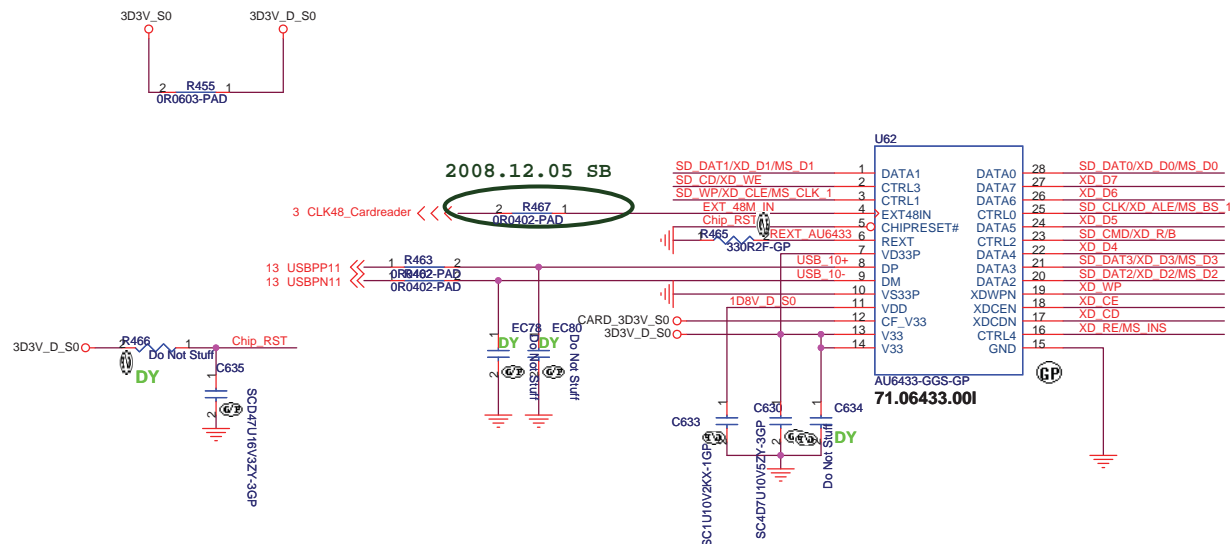
Rev

JM70-MV

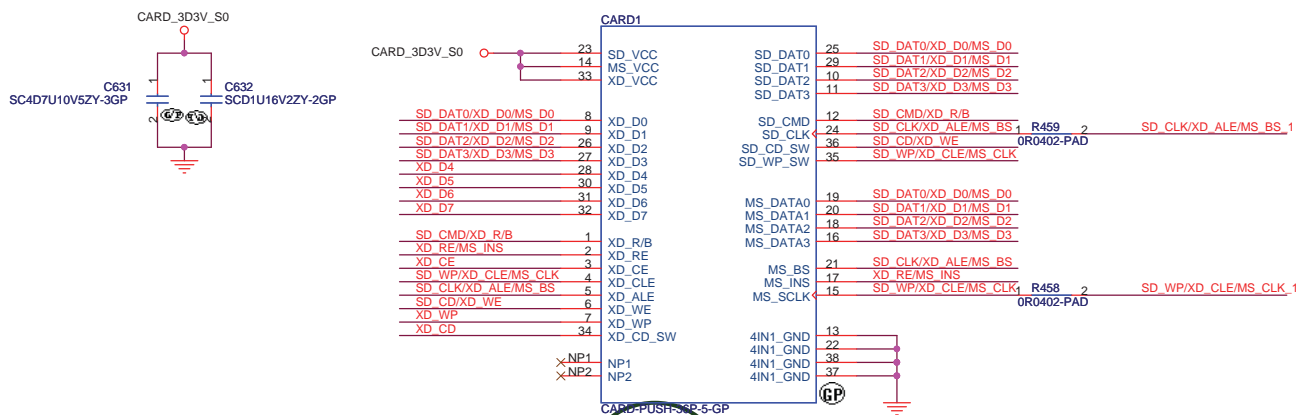
SB

Date: Saturday, December 20, 2008

Sheet	34	of	55
-------	----	----	----



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)

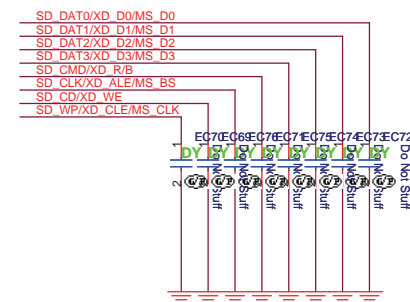


2nd = 20.10079.011

20.10081.011

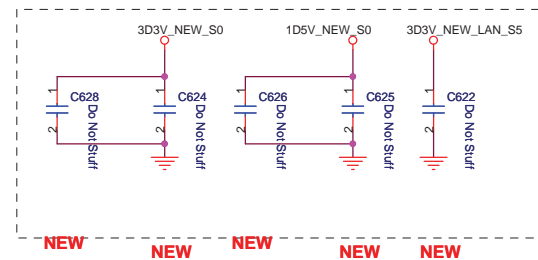
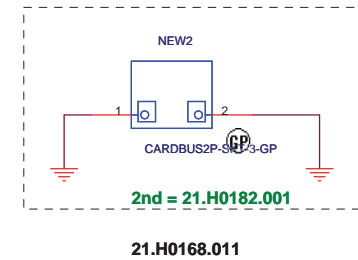
2008.12.12 SB

EMI capacitor



UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: Cardreader			
Size	Document Number	Rev	SB
Date: Saturday, December 20, 2008	Sheet 35 of 55	JM70-MV	

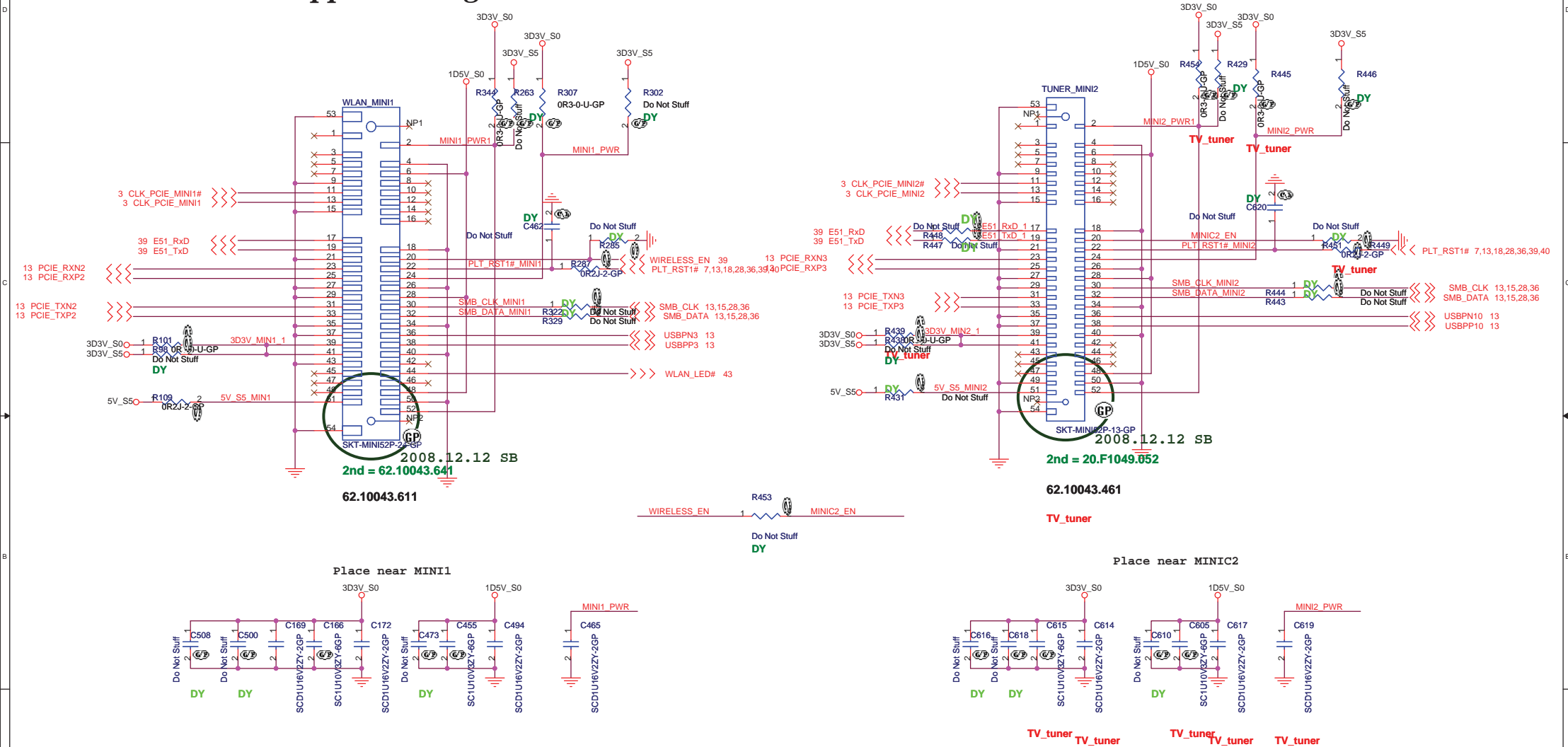


Sheet	36	of	55
-------	----	----	----

Mini1 Card Connector(WLAN)

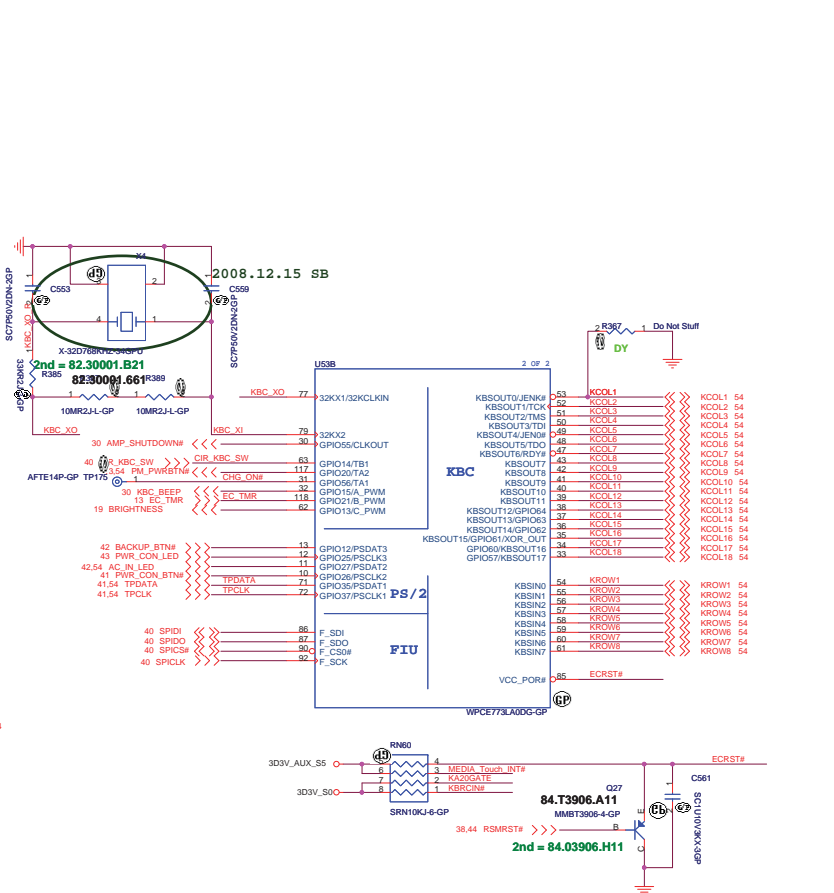
Support debug-card

Mini2 Card Connector(TV tuner)





RSET = 0.0012T2 - 0.9308T + 96.147
T8 seting 90 degree



2008.12.08 SB

2nd = 20.K0326.026

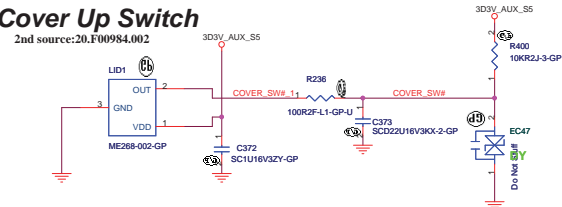
KB1
PTWO-C0826-1-GP

20.K0326.026

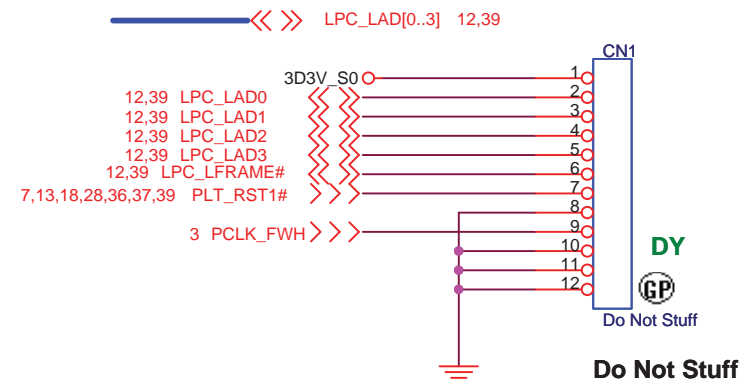
27 28

K00L1 K00L2 K00L3 K00L4 K00L5 K00L6 K00L7 K00L8 K00L9 K00L10 K00L11 K00L12 K00L13 K00L14 K00L15 K00L16 K00L17 K00L18 K00L19 K00L20 K00L21 K00L22 K00L23 K00L24 K00L25 K00L26

K01 K02



VISHAY CIR Module

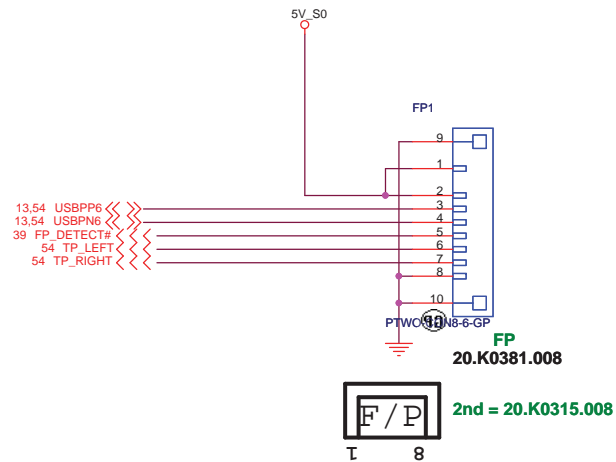


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

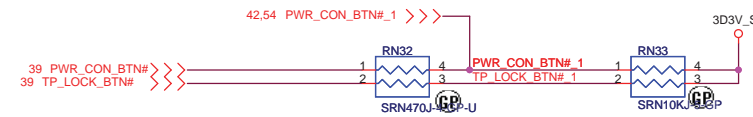
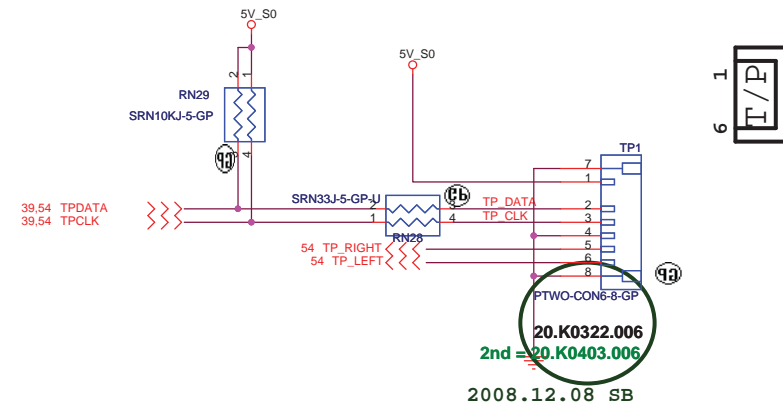
Size	Document Number	Rev
	JM70-MV	SE

Date: Saturday, December 20, 2008 Sheet 40 of 55

Finger printer

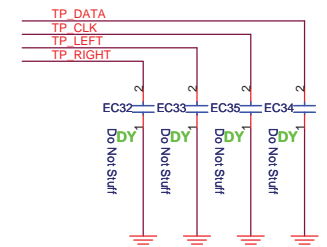
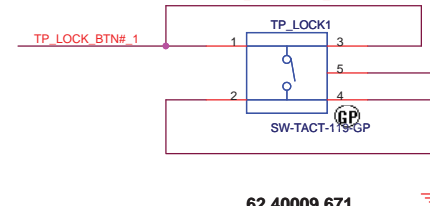


Touch Pad



TP_LOCK key

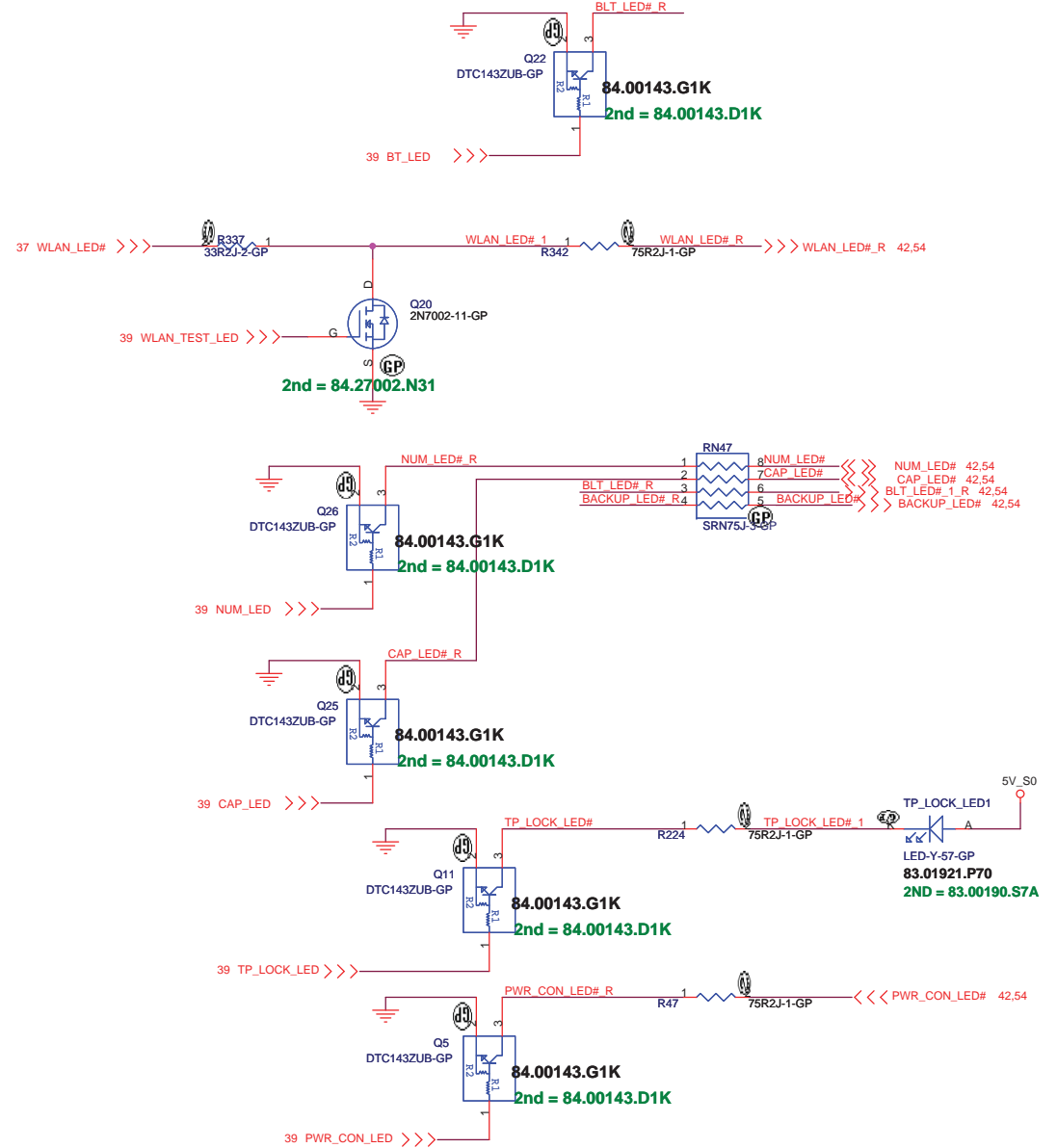
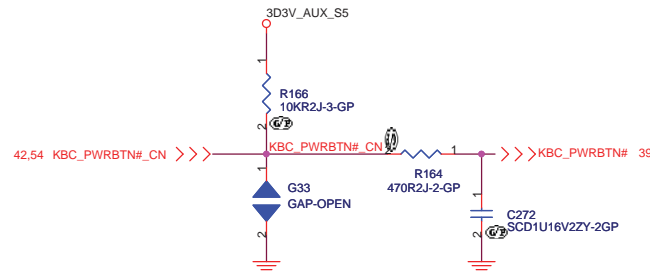
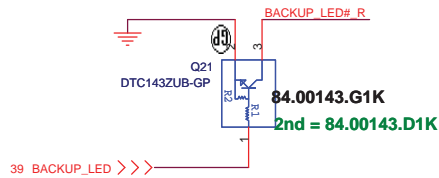
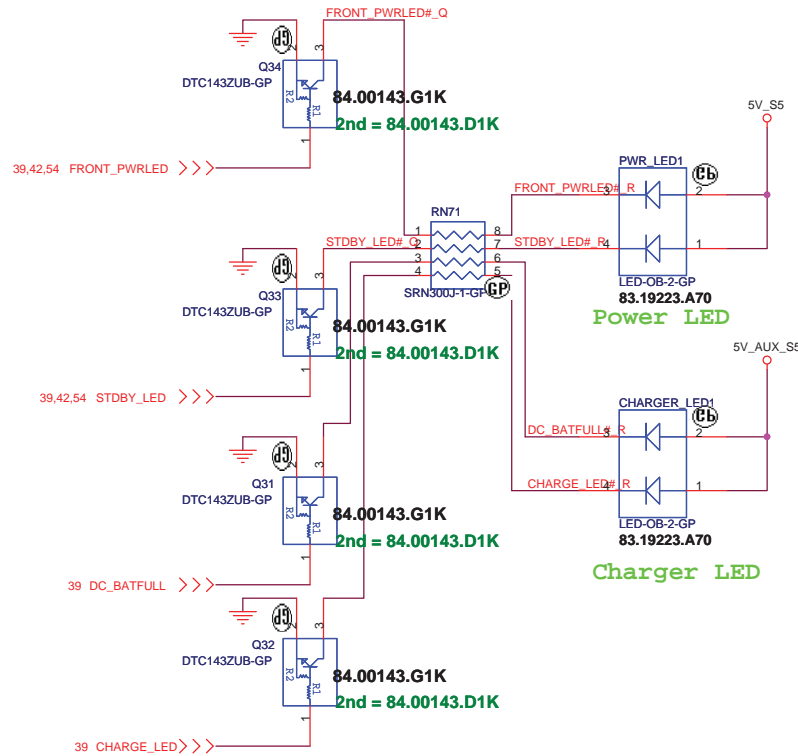
Note. main with 2nd symbol pin define different



UMA

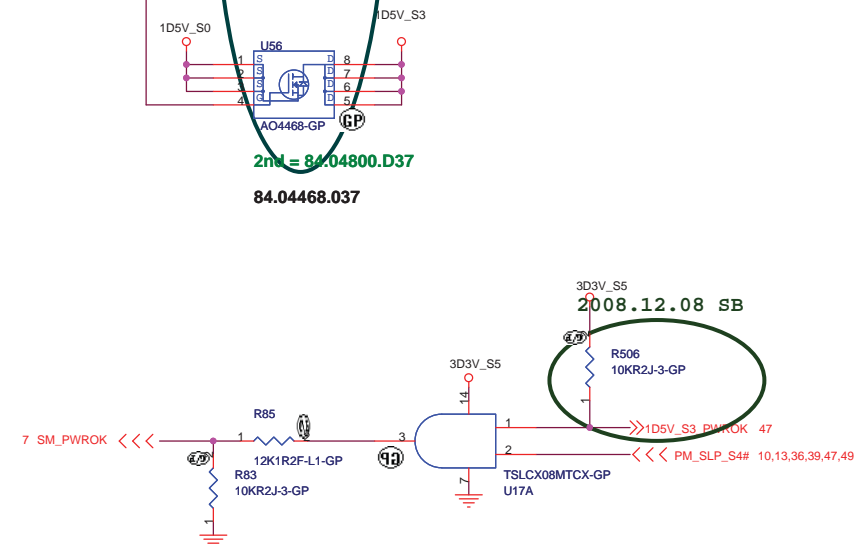
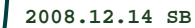
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title Touch PAD and FP			
Size	Document Number		Rev
	JM70-MV		SB
Date:	Saturday, December 20, 2008	Sheet	41 of 55

LED



UMA

3D3V_AUX_S5



2008.12.08 SB

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

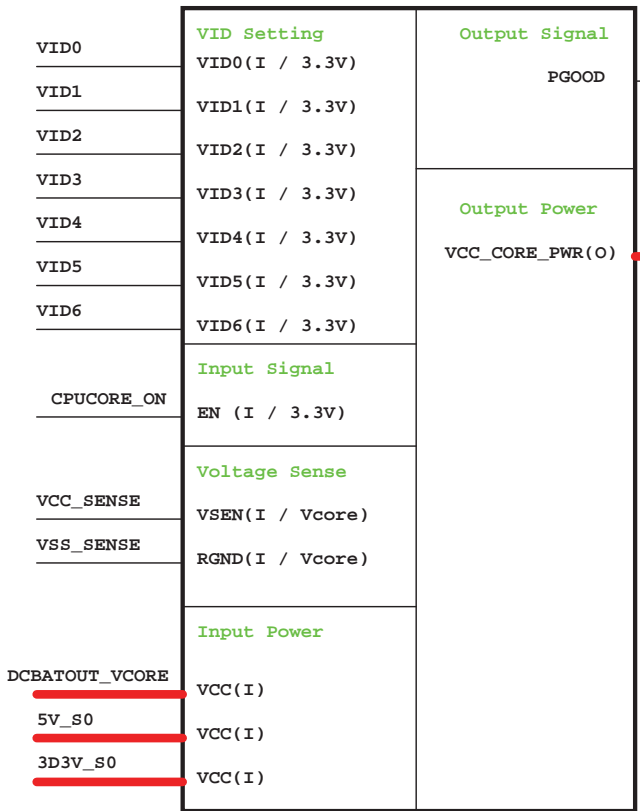
Title	<i>RUN POWER and 3D3V_AUX_S5</i>
-------	---

Size	Document Number	Rev
------	-----------------	-----

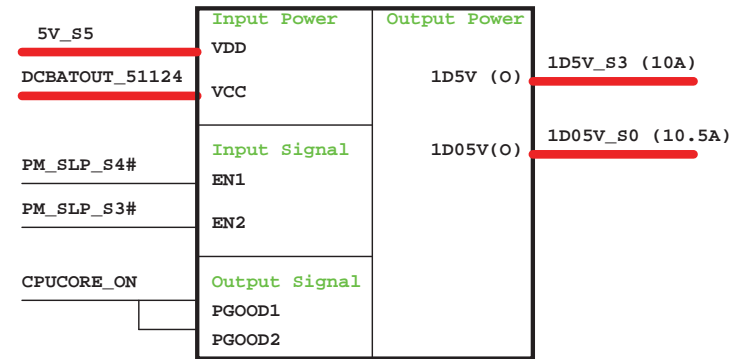
IM70-MV SB

Date: Saturday, December 20, 2008 Sheet 44 of 55

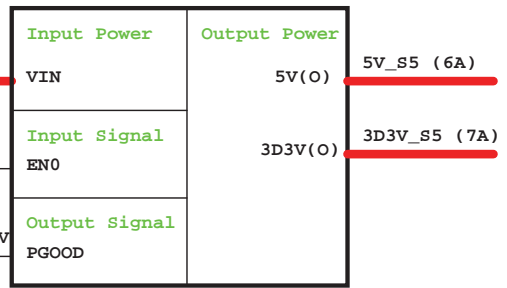
CPU_CORE
ADP3208C



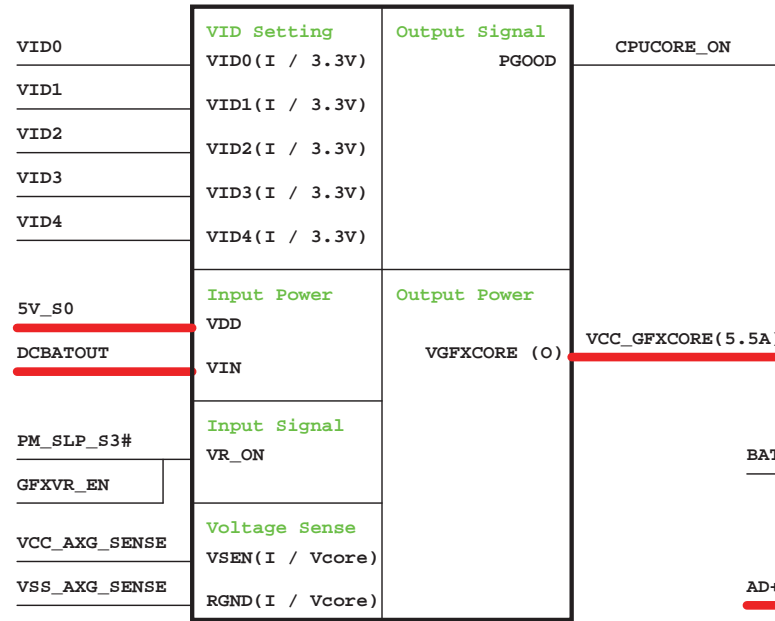
TPS51124
1D5V/1D05V



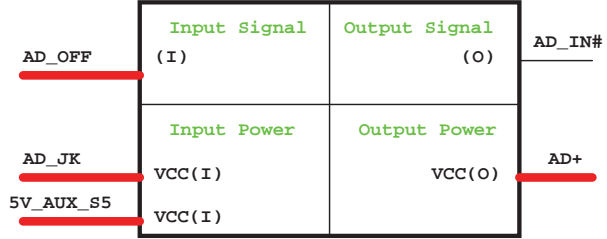
ISL62392
5V/3D3V



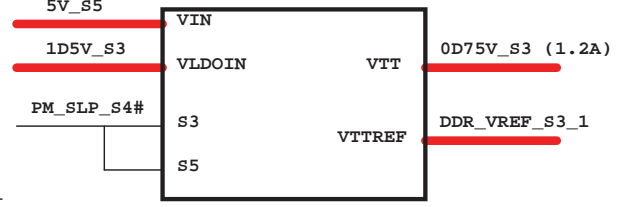
GFX_CORE
ISL6263A



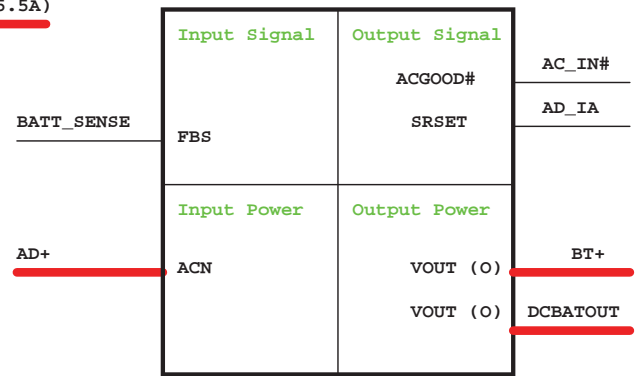
Adapter



DDR 3.0
RT9026 0D75V_S0

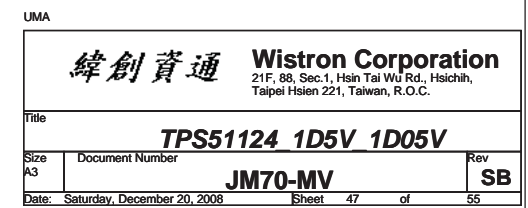


Charger ISL88731A

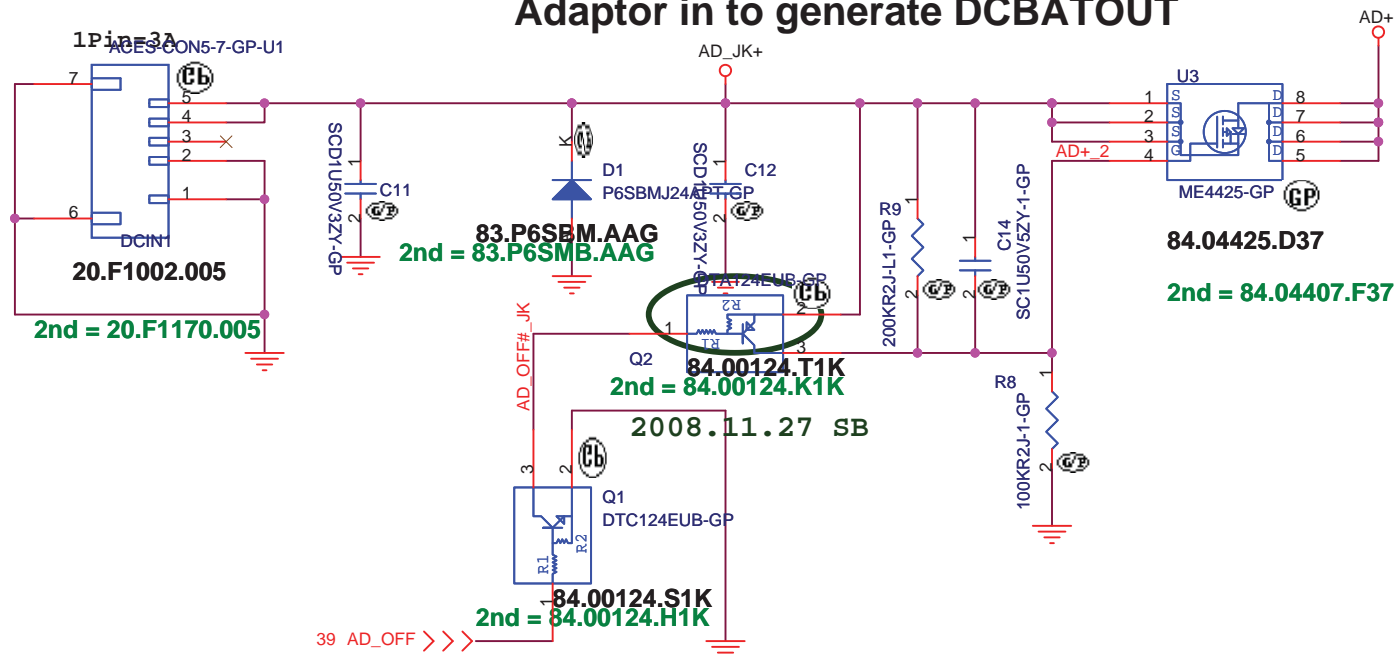


UMA

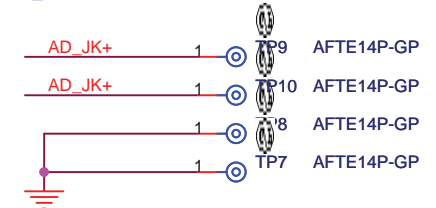
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Power Block Diagram	
Size B	Document Number
JM70-MV	
Date: Saturday, December 20, 2008	Sheet 45 of 55



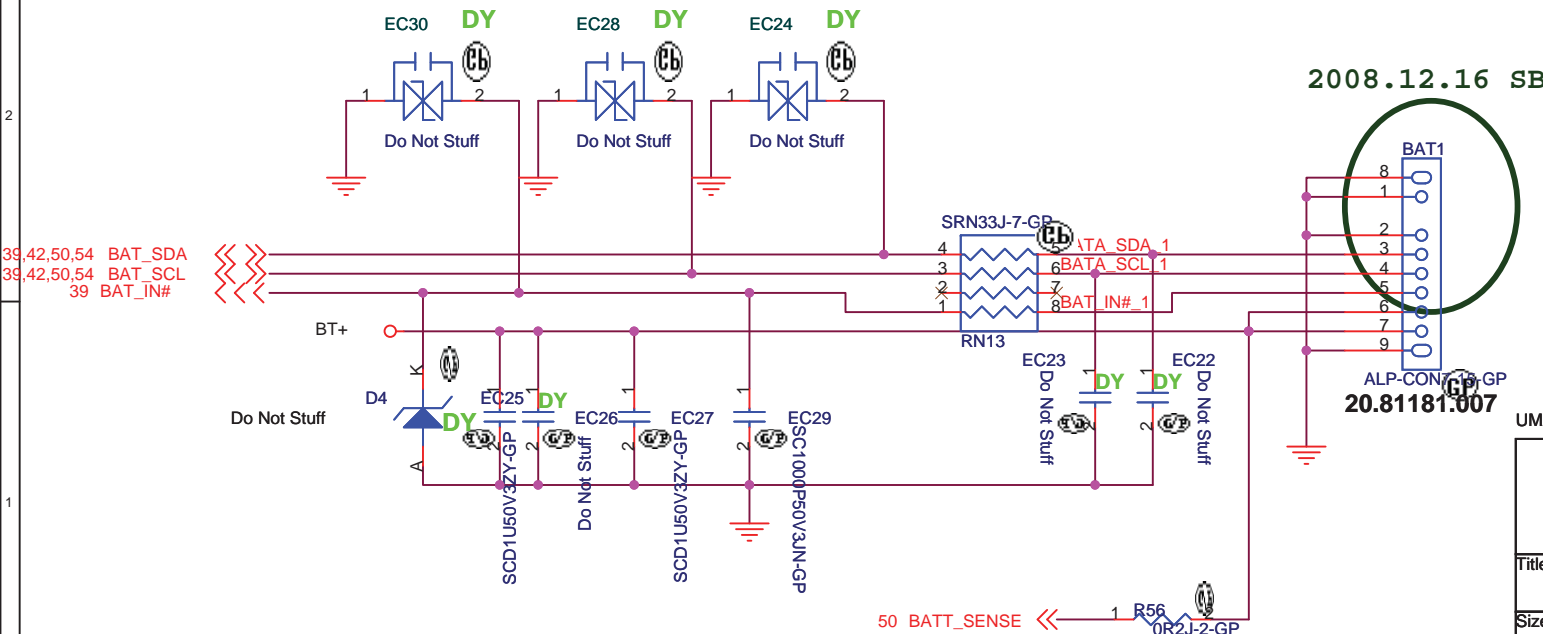
Adaptor in to generate DCBATOUT



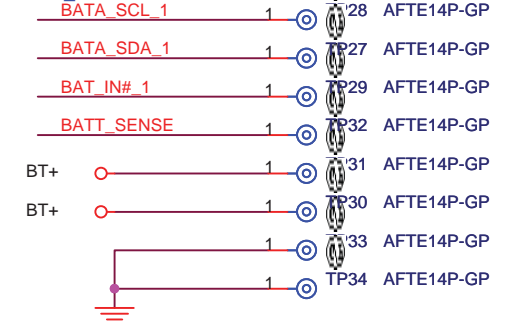
KB Conn. Test Point
keep on connector side



MAIN BATTERY CONNECTOR

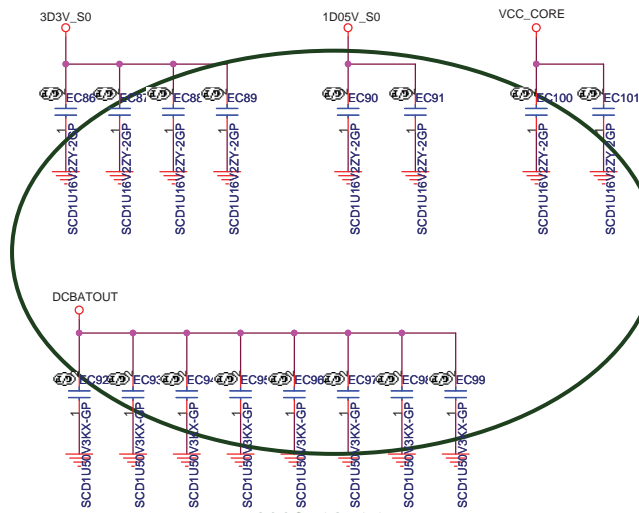
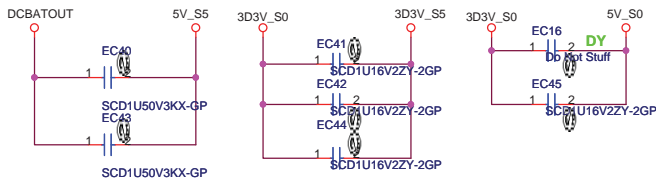


BAT1 Conn. Test Point
keep on connector side

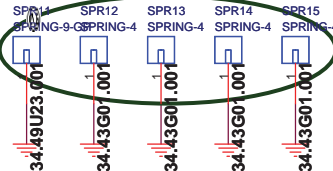
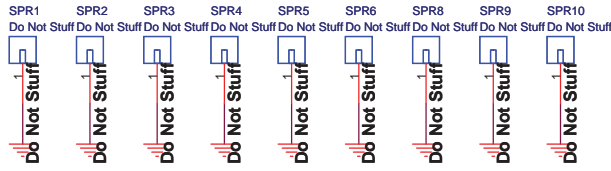


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				
AD&BTY CONNECTER				
Size	Document Number			Rev
JM70-MV			SB	
Date:	Saturday, December 20, 2008		Sheet 52 of 55	

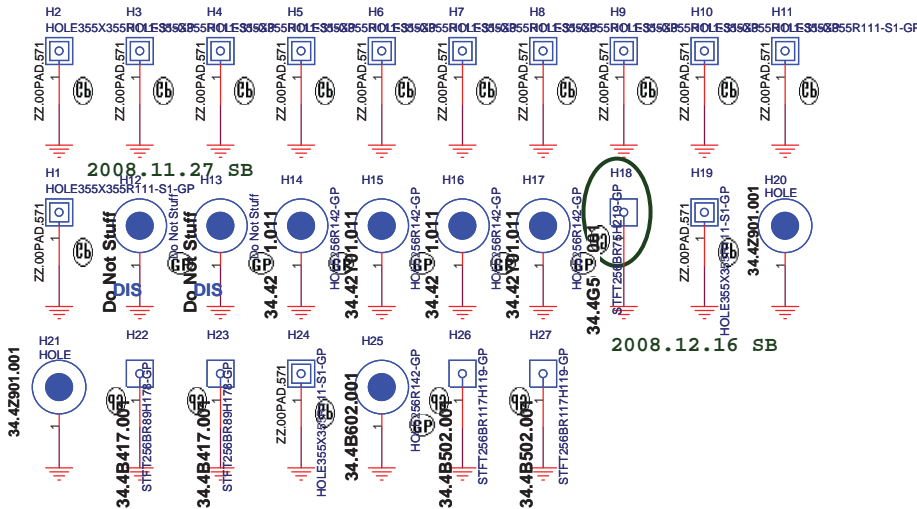


2008.12.16 SB

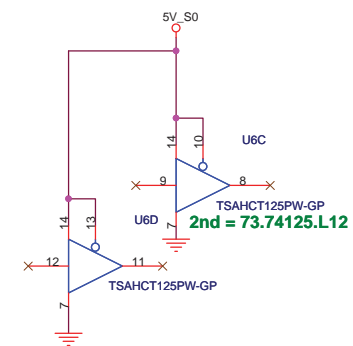
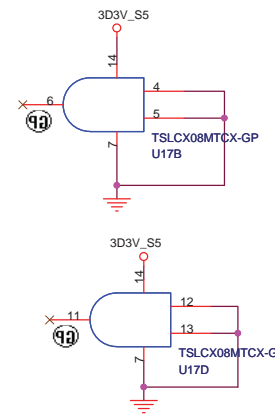


2008.12.16 SB

DY DY DY DY DY DY DY DY DY

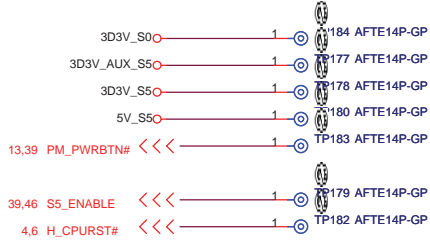


2008.12.16 SB



2nd = 73.74125.L12

Check test point



Test Point放在Dimm Door打開可量測處

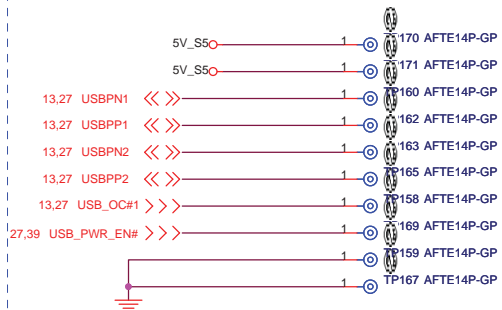
CCD_DMIC_CN1 Conn. Test Point keep on connector side



BT Conn. Test Point keep on connector side



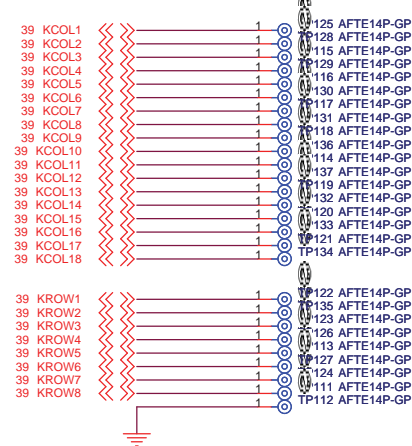
USB_CN1 Conn. Test Point keep on connector side



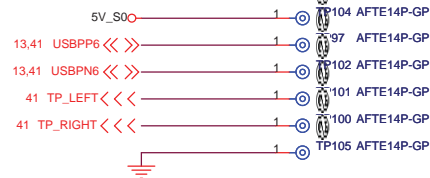
SPKR1 Conn. Test Point keep on connector side



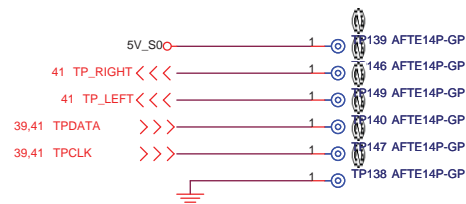
KB1 Conn. Test Point keep on connector side



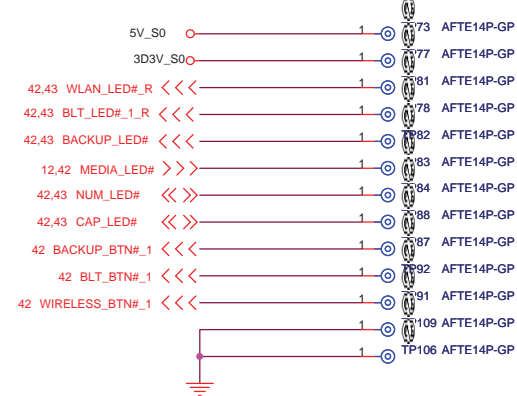
FP test Point keep on connector side



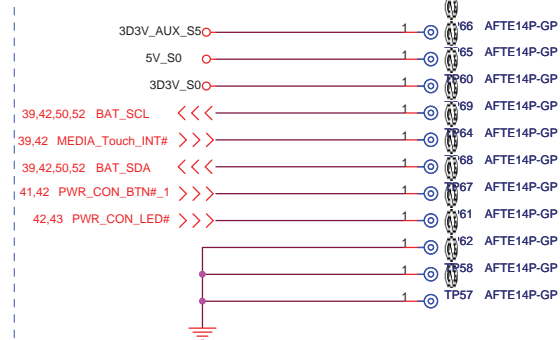
TOUCH PAD Conn. Test Point keep on connector side



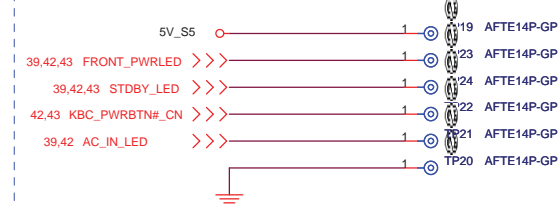
LAUN_CN1 Conn. Test Point keep on connector side



PWR_SAVING_CN1 Conn. Test Point keep on connector side



PWR_BT_CN1 Conn. Test Point keep on connector side



UMA

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		AFTE TP	
Size	Document Number	Rev	
A3	JM70-MV	SB	
Date:	Saturday, December 20, 2008	Sheet	54 of 55



UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY

Size
A2

Document Number
JM70-MV

Rev
SB

Date: Saturday, December 20, 2008

Sheet 55 of 55